Module 4

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Oscillators

4.0 Relaxation (Square Wave) Oscillators

What you´ll learn in Module 4

Relaxation (Square Wave) Oscillators

There are a number of oscillator designs that produce square waves at frequencies from less than 1Hz to several GHz. Square waves are used to control the timing of operations in digital systems, such as clock generators for microprocessors. They also have many uses in analogue circuits from simple lamp flashers to complex control systems as well as pulse width control systems for audio and radio applications.

These different circuits go under a variety of names, such as:

Astable oscillators

This name comes from the fact that these oscillators have no stable state; their output changes repeatedly from high to low and back to high.

Astable multivibrators

Some astables consist of more than one (e.g. two oscillating amplifiers).

Aperiodic Oscillators

Because they are untuned oscillators.

Clock Oscillators

In digital applications the main function of these oscillators is the production of square wave outputs, or pulse trains.

Square wave oscillators can also be used as the basis for sawtooth oscillators or sweep generators.

Properties of Square Waves

Square waves may be perfectly symmetrical with the height and width of both the mark and the space being equal, but this is not necessarily the case. Where the mark and the space are of equal width (time), the waveform is said to have a mark to space ratio of 1:1 but in the lower waveform in Fig. 1 the mark is twice the width of the space and so the mark to space ratio is 2:1.

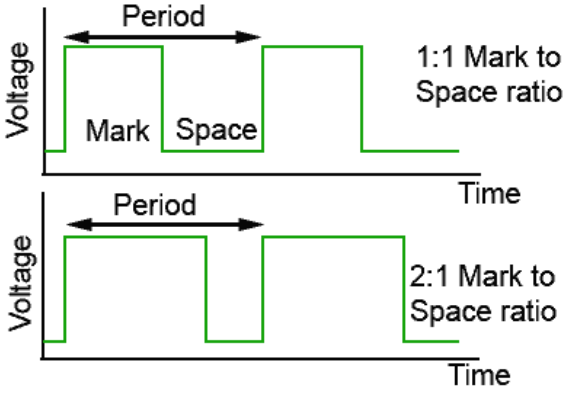

Fig. 4.0.1 Mark to Space Ratio

The height (Voltage) of the mark does not need to be equivalent to its width, provided that the voltage and timing of the waveform is known.

Waveforms of a rectangular rather than square shape can also be considered square waves.

Where the time of the mark is much shorter than that of the space however, the waveform is more properly called a series of pulses or a pulse train as shown in Fig. 4.0.2.

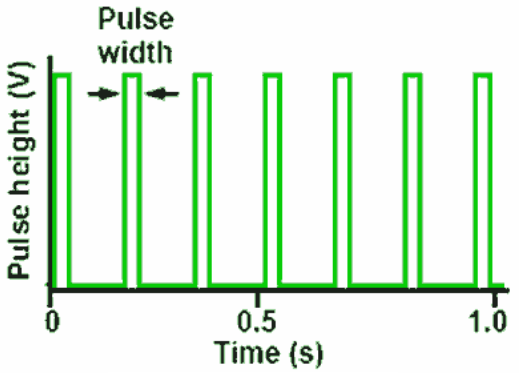

Fig. 4.0.2 Pulse Train

With pulses the frequency of the wave is more usually referred to as the "Pulse repetition frequency" (p.r.f.), which refers to the number of pulses occurring in one second rather than the more usual Hz or cycles per second.

A square wave is a complex wave, meaning that unlike the sine wave, which has only a single sine component, it is made up of many sine wave components. It has a 'fundamental', a sine wave of the same amplitude and frequency as the square wave, plus, in a perfect square wave, an infinite number of odd harmonics. This means that to produce a perfect square wave, the oscillator and any circuits being fed by it, must have an infinitely wide bandwidth, with constant gain over the whole bandwidth. As this level of perfection is not practicable, it is to be expected that some distortion of the square wave will be present. Figs 4.0.3, 4 and 5 illustrate some commonly encountered distortions to square waves.

Rise and Fall Time

Fig. 4.0.3 shows a square wave in which the vertical edges are not vertical. The rise and fall in voltage should be instantaneous but here there is a distinct lengthening of the rise and fall times plus a certain amount of rounding of the waveform. This is typical of poor high frequency response in an oscillator or amplifier circuit, the higher frequency harmonics are reduced or missing, also causing a 'rounding' of the waveform. A similar effect, but without the rounding can be evident at higher frequencies in op amp astables due to slew rate limiting.

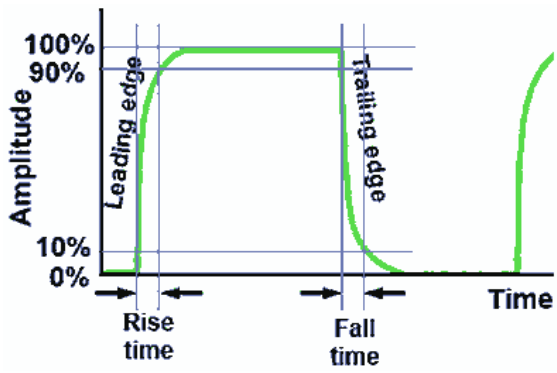

Fig. 4.0.3 Slow Rise & Fall Times

Ringing

Fig. 4.0.4 Illustrates 'Ringing' following the vertical transitions of the wave, this may be caused by the presence of stray inductance and capacitance in the circuit causing damped oscillations to begin at some high frequency, together with large high frequency gain.

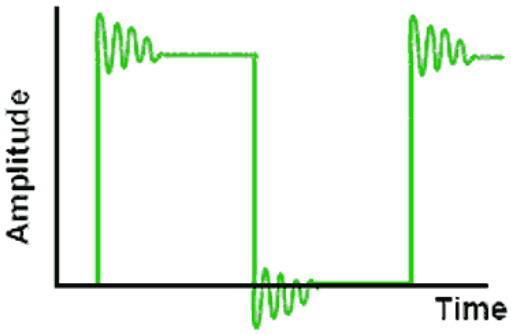

Fig. 4.0.4 Ringing

Overshoot

Fig. 4.0.5 illustrates 'Overshoot' where the rising and falling edges of the wave continue above and below the maximum amplitude of the wave. Overshoot is generally measured as a percentage of the total (normal) amplitude of the wave. It may be caused by the presence of stray inductance creating excessive high frequency gain.

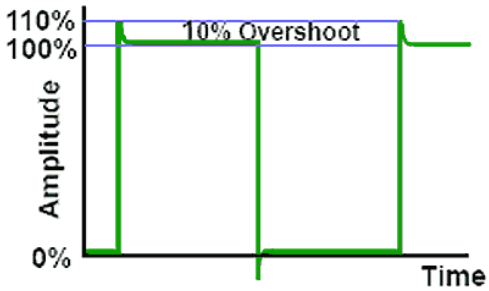

Fig. 4.0.5 Overshoot

Oscillators – Module 4

4.1 BJT Astable Multivibrators

What you'll learn in Module 4.1

After studying this section, you should be able to:

- Recognise BJT astable multivibrator circuits.
- Understand the operation of astable multivibrators.
- Calculate the frequency of an astable multivibrator.
- Understand methods for varying the frequency and mark to space ratio of the output wave.

BJT Astable Multivibrators

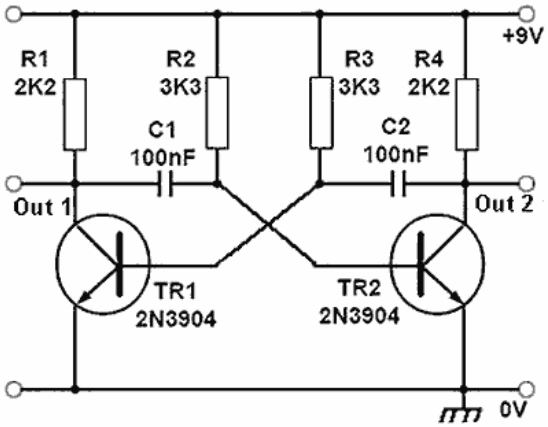

Fig. 4.1.1 Basic BJT Astable Multivibrator

The basic bipolar transistor (BJT) version of an astable multivibrator as shown in Fig. 4.1.1 has two outputs that repeatedly change state at a rate determined by the time constants of its feedback network. Although largely superseded by its equivalent op amp or timer IC versions in many applications, it is still a useful and flexible design for square wave and pulse generation.

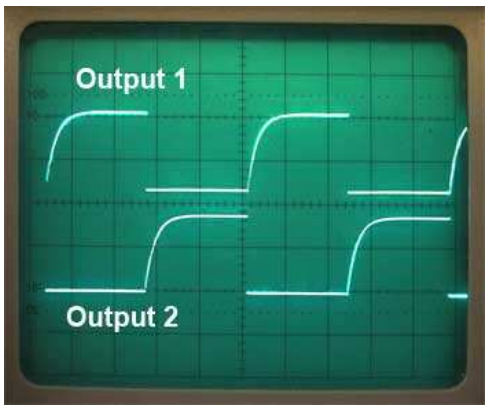

Fig. 4.1.2 Antiphase Outputs

The circuit switches continuously from one state (TR1 on and TR2 off) to the other (TR1 off and TR2 on) and back again at a rate determined by the RC timing components Cl/R2 and C2/R3. The circuit produces two anti-phase square wave signals, with an amplitude almost equal to its supply voltage, at its two transistor collectors as shown in Fig 4.1.2.

Astable Operation

Suppose that at switch on, TR1 is conducting heavily and TR2 is turned off. The collector of TR1 will be almost at zero volts as will the left hand plate of C1. Beause TR2 is turned off at this time, its collector will be at supply voltage and its base will be at almost zero potential, the same as TR1 collector, because C1 is still un-charged and its two plates are at the same potential.

C1 now begins to charge via R2 and its right hand plate becomes increasingly positive until it reaches a voltage of about +0.6V. As this plate of the capacitor is also connected to the base of TR2, this transistor will begin to conduct heavily. The rapidly increasing collector current through TR2 now causes a voltage drop across R4, and TR2 collector voltage falls, causing the right hand plate of C2 to fall rapidly in potential.

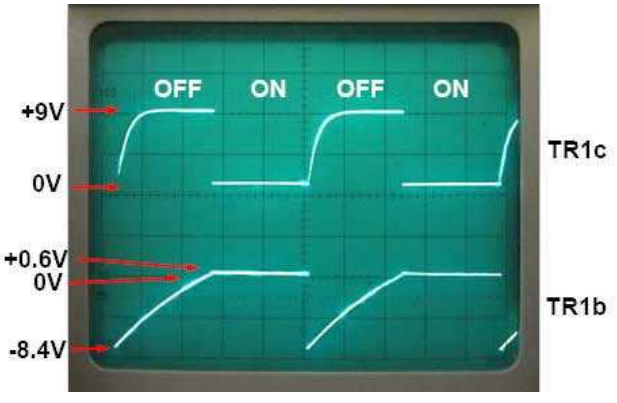

Fig. 4.1.3 Switching Action (on TR1)

It is the nature of a capacitor that when the voltage on one plate changes rapidly, the other plate also undergoes a similar rapid change, therefore as the right hand plate of C2 falls rapidly from supply voltage to almost zero, the left hand plate must fall in voltage by a similar amount.

With TR1 conducting, its base would have been about 0.6V, so as TR2 conducts TR1 base falls to 0.6 −9V = −8.4V, a negative voltage almost equal and opposite to that of the +9V supply voltage.

This rapidly turns off TR1 causing a rapid rise in its collector voltage. Because a **sudden** voltage change on one plate of a capacitor causes the other plate to change by a similar amount, this sudden rise at TR1 collector is transmitted via C1 to TR2 base causing TR2 to rapidly turn on as TR1 turns off. A change of state has occurred at both outputs.

This new state does not last however. C2 now begins to charge via R3, and once the voltage on the left hand plate (TR1 base) reaches about +0.6V another rapid change of state takes place. This switching action produces the collector and base waveforms shown in Fig. 4.1.3.

The circuit keeps on changing state in this manner producing a square wave at each collector. The frequency of oscillation can be calculated, as the time for the relevant capacitor to charge sufficiently for a change of state to take place, will be approximately 0.7CR and, as two changes of state occur in each cycle the periodic time T will be:

$$T = 1.4(C1R2+C2R3)$$

If C1 = C2 and R2 = R3 the mark to space ratio will be 1:1and in this case the frequency of oscillation will be:

$$f_o = \frac{1}{1.4CR}$$

Example

What is the frequency of an astable multivibrator of mark/space ratio 1:1 using timing components of C=100nF and R=33K?

$$f_o = \frac{1}{1.4CR}$$

$$= \frac{1}{1.4 \times 100\text{exp}^{-9} \times 33\text{exp}^{3}}$$

$$= 216\text{Hz}$$

Improving Rise Times

A problem with the basic astable circuit is that the capacitor action described above slows down the rise in voltage as each transistor turns off, producing the curved rising edges to the square wave as can be seen in Fig. 4.1.2. This can be overcome by the modified circuit shown in Fig. 4.1.4

Each time TR2 collector voltage goes high as the transistor turns off, D2 becomes reverse biased, isolating TR2 from the effect of C2 charging.

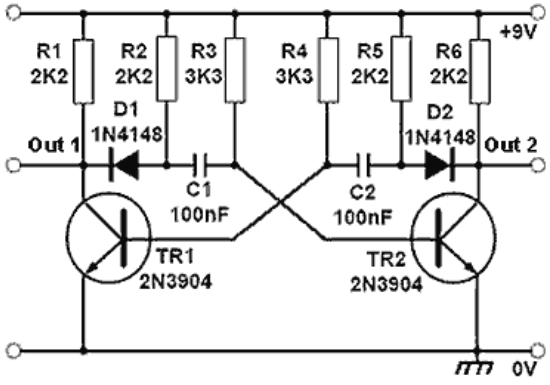

Fig. 4.1.4 BJT Astable Modified for Improved Rise Time

The charging current for C2 is now supplied by R5 instead of R6. The action of TR1 during its 'off' period is similar.

The output waveforms at the collectors of TR1 and TR2 shown in Fig. 4.1.5 demonstrate the improved rise times achieved by the modified circuit of Fig. 4.1.4, compared with those for the basic BJT astable circuit shown in Fig. 4.1.2.

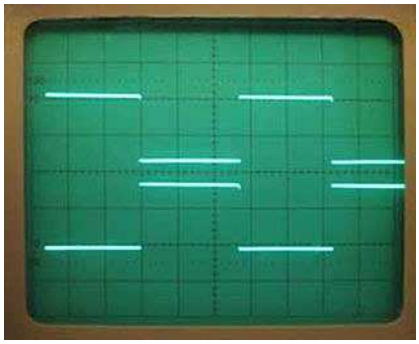

Fig. 4.1.5 Astable Output Showing Improved Rise Time

Variable Frequency Astable

It is useful to be able to vary the frequency of operation, and this may be done as shown in Fig.4.1.6.

By varying VR1 the voltage at the top of both R3 and R4 is varied so that whatever mark to space ratio is used, only the frequency alters, whilst the mark to space ratio is maintained.

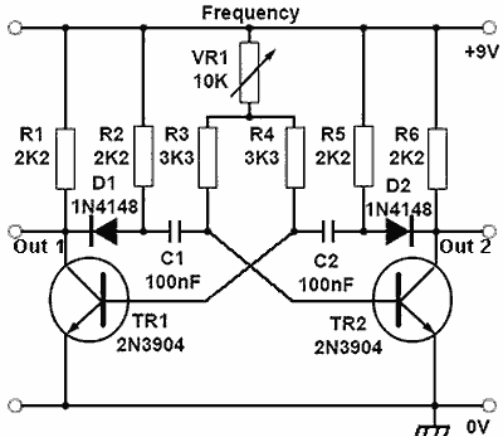

Fig. 4.1.6 Variable Frequency BJT Astable

Variable Mark to space Ratio

Fig. 4.1.7 shows how by using a potentiometer instead of a variable resistor, an astable with a degree of variable mark to space ratio can be achieved.

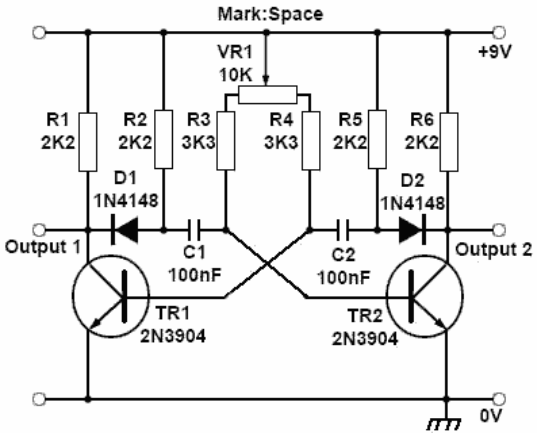

Fig. 4.1.7 Variable Mark to Space Ratio Astable

Oscillators – Module 4
4.2 Op-amp Astables

What you'll learn in Module 4.2

After studying this section, you should be able to:

- Understand the operation of astable oscillators using op-amps.
- Describe the limitations due to Slew Rate.
- Calculate the frequency of an op-amp astable.
- Describe methods for changing the frequency and mark to space ratio of op-amp astables.

How Op Amp Astables Work

Astables can be constructed around op amps and may use fewer components than the BJT designs described in Oscillators Module 4.1. Op amp designs are very useful, especially at low frequencies; at higher frequencies however, unless high-speed op amps are used a problem occurs, as many standard (and older design) op amps are not able to handle the very fast voltage transitions required for good square wave shape, due to slew rate limiting.

The slew rate of an op amp is measured in V/µs (Volts per microsecond), and the output voltage of an astable must be able to change very rapidly by almost the full amount of the supply voltage as the output switches from low to high or back to its low level. However, a typical slew rate for many popular op amps may be around 0.5V/µs and such an op-amp would therefore would take 36µs for the output voltage to change by the 18V between –9V to +9v on a standard dual supply.

Fig. 4.2.1 shows this may not be a problem in a low frequency astable; for example the 36µs rising edges and falling edge would occupy 72µs, just 0.72% of the 10ms periodic time of a 100Hz square wave. However in a 5kHz square wave, having a periodic time of only 200µs the slopes of the rising and falling edges would occupy 36% of the whole cycle of the wave.

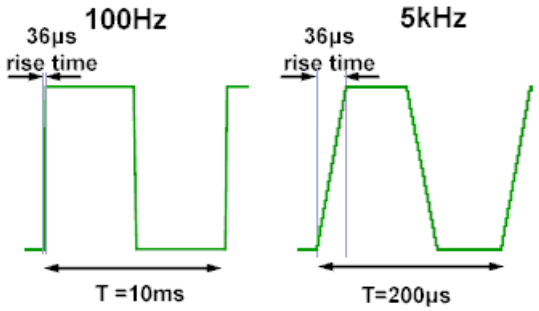

Fig. 4.2.1 The Effect of Slew Rate on Square Waves

Reducing the supply voltage would help overcome this problem to some extent, but a better solution is to use a high-speed op amp, which will have slew rate in excess of 10V/µs. A number of op amps fit this specification and some may also operate from a single power supply of 3V or less. Using comparators, which have a much faster response time (the term 'slew-rate' is not really applicable to comparators) than standard op-amps is also a good option for higher frequency designs.

Fig. 4.2.2 shows a basic astable circuit using a LM324 operating from a single +9V supply, and suitable for generating square wave or pulse signals up to a frequency of about 2kHz. The operation of the circuit relies on repeatedly charging and discharging C1 from the output of the op amp via R5; these two components therefore set the operating frequency of the oscillator.

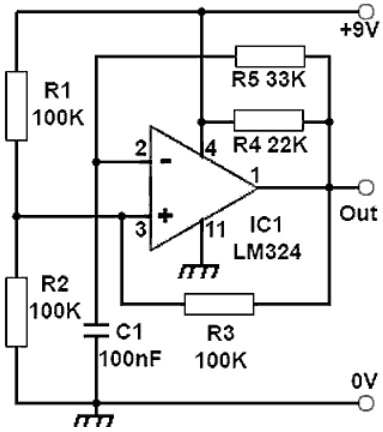

Fig. 4.2.2 Basic Op-amp Astable

R1, R2 and R3 control the maximum and minimum voltage that C1 charge attains during a cycle of oscillation, and the purpose of R4 is to force the class B output of the LM324 into class A to avoid any crossover distortion in the output waveform as described in Oscillators Module 3.4.

Astable Circuit Operation

Assuming the output (pin 1 of IC1) of the LM324 in Fig. 4.2.2 is at the supply voltage of (+9V), R1, R2 and R3 can be considered to be connected as shown in Fig. 4.2.3a where R1 and R3 are connected in parallel and therefore have an effective resistance of:

100KΩ/2 = 50KΩ

As this parallel resistance of 50KΩ forms a potential divider with R2(100KΩ) and with a supply of +9V the voltage at the centre point of the divider will be 2/3 of 9V = 6V. While the output is high C1 will be charging at a rate determined by R5 towards +9V.

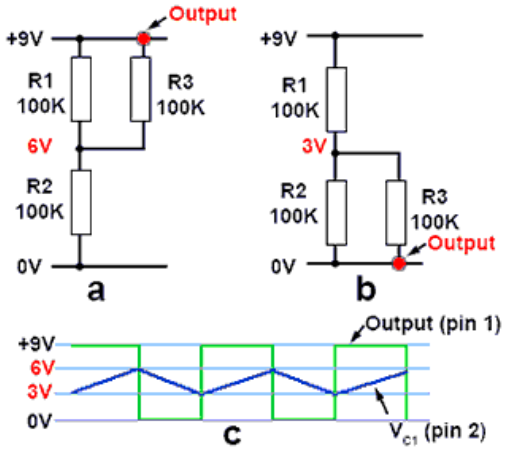

Fig. 4.2.3 Astable Circuit Operation

Once the capacitor (also connected to pin 2 of IC1) reaches a voltage of 6V however, it will exceed the voltage on pin 3, and the amplifier, due to its high gain, will act as a comparator and its output will immediately change to 0V.

The output end of R3 is therefore now connected to 0V creating the condition illustrated in Fig. 4.2.3b. The potential on pin 2 of IC1 is now 3V and the capacitor will be discharging via R5 towards the new output potential of 0V. On discharging past 3V however, pin 2 of IC1 becomes less than pin 3 and the amplifier output returns to +9V, completing one whole cycle.

The action repeats, generating a square wave at pin 1 of about 8Vpp and a 3Vpp triangular wave at pin 2 of the op amp. The actual waveforms produced by this circuit are shown in Fig. 4.2.4.

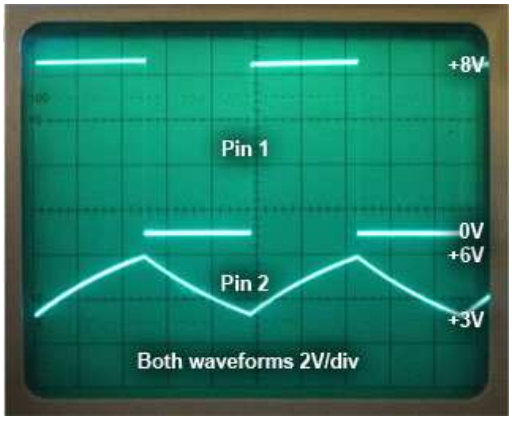

Fig. 4.2.4 Astable Circuit Waveforms

With the component values shown in Fig. 4.2.2 the circuit oscillates at a frequency slightly above 200Hz. The formula relating the frequency of oscillation, to the values of R5 and C1, allowing for the partial charge and discharge of C1 is therefore:

$$f_o = \frac{1}{2(\ln 2) \times RC}$$

or

$$f_o = \frac{1}{1.386 \times RC}$$

Note: The natural log (ln) of 2 is often shown as 1.4 rather than 1.386

This formula for frequency only remains reasonably accurate however while the rise and fall times of the wave are much shorter than the periodic time of the wave giving virtually vetrtical rising an falling edges to the square wave. Therefore there can be an increasing discrepancy between the calculated and actual frequency of the oscillator at higher frequencies as any limitations of slew rate increase.

Modifications to the Basic Astable

Variable Frequency

In Fig. 4.2.5, R5 has been replaced with a 100K variable resistor to make the frequency of oscillation variable. The choice of value for VR1 depends on the frequency range required. An additional fixed resistor could be added in series with VR1 if required to limit the minimum resistance.

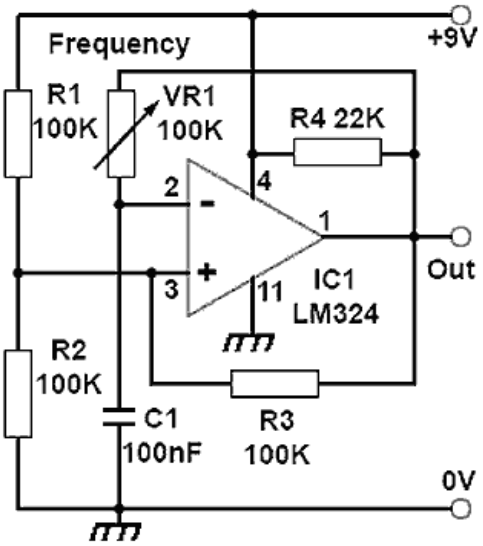

Fig. 4.2.5 Variable Frequency Op-Amp Astable

Low Frequency LED Flasher

Fig. 4.2.6 shows a low frequency square wave oscillator suitable for driving flashing LEDs. The output of the LM324 is easily capable of providing sufficient current to drive LEDs and this arrangement will source about 10mA to drive D2 when the output is high, and will sink (conduct to ground) the same amount of current when the output is low, to drive D1 from the supply. The frequency may be fixed, using a 33K fixed resistor as in Fig. 4.2.2, or variable using a variable resistor as in Fig. 4.2.6. At low frequencies, a much higher value for C1 is required and therefore an electrolytic capacitor is used. Careful attention must be given to correct polarity when constructing the circuit, and to avoid sudden capacitor failure, a component should be chosen that has a working voltage higher than the supply voltage. However as electrolytic capacitors do not work correctly as capacitors at less than 10% of their rated voltage, the working voltage should ideally not be more than 10 times the supply voltage.

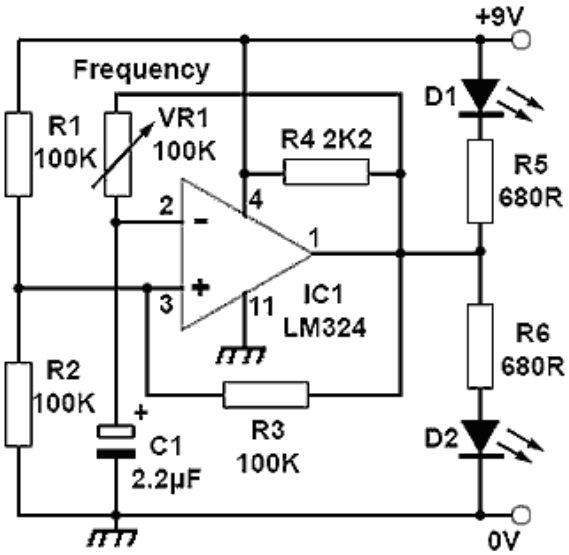

Fig. 4.2.6 Low Frequency LED Flasher

Varying the Mark to space Ratio

Fig. 4.2.7 illustrates a method of generating variable width pulses without affecting the frequency. In this circuit a mark to space ratio control (VR1) and two opposing polarity diodes D1 and D2 form the resistive part of the CR time constant. With VR1 wiper at a central position, a 1:1 mark to space ratio is obtained. When IC1 pin 1 is high, D2 conducts making the lower half of VR1 the active resistor in the CR time constant. When IC1 pin 1 is low, D1 conducts and the upper portion of VR1 is used in the CR time constant. Varying VR1 wiper will provide differing values of resistance during the on and off periods of the waveform, effectively providing either positive going or negative going 9Vpp pulses at the output that can be used for many purposes including PWM (pulse width modulation) for lighting or motor control.

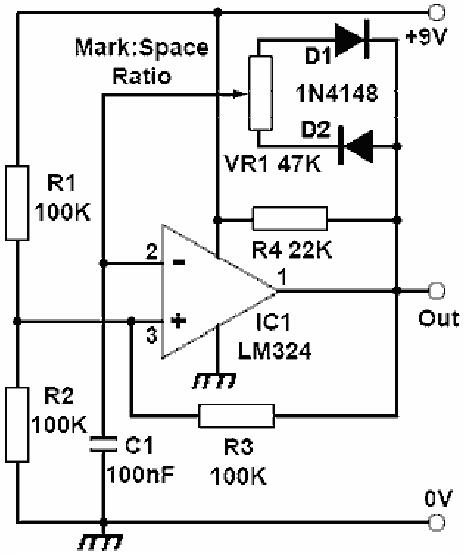

Fig. 4.2.6 Variable Mark to Space Ratio Astable

Oscillators – Module 4
4.3 555 Astables

What you'll learn in Module 4.3

After studying this section, you should be able to:

- Understand the basic operation of a 555 timer.
- Understand the operation of a 555 timer in astable mode.
- Understand time constants in a 555 timer.
- Calculate the frequency of a 555 timer in astable mode.

Astable Oscillators Using the 555 Timer

A popular way of implementing an astable square wave oscillator is to use the 555 Timer IC. This is one of the most commonly available Timer ICs and has many different uses. As well as being used to construct astable oscillators, it can also be used in monostable mode where an input pulse is used to trigger a time delay set by an RC time constant, during which the output pin goes to a high level (+Vcc) and then returns to 0V to await a further trigger pulse at the IC input pin.

The 555 Timer IC

The 555 in its astable configuration can be used to generate a square wave signal with a number of variations:

- Square wave with even or uneven mark to space ratio
- Pulse train
- Pulse width modulation
- Pulse position modulation
- Frequency modulation

The internal component parts of the 555 Timer IC together with the IC pin out are illustrated in Fig. 4.3.1, the function of the pins are as follows:

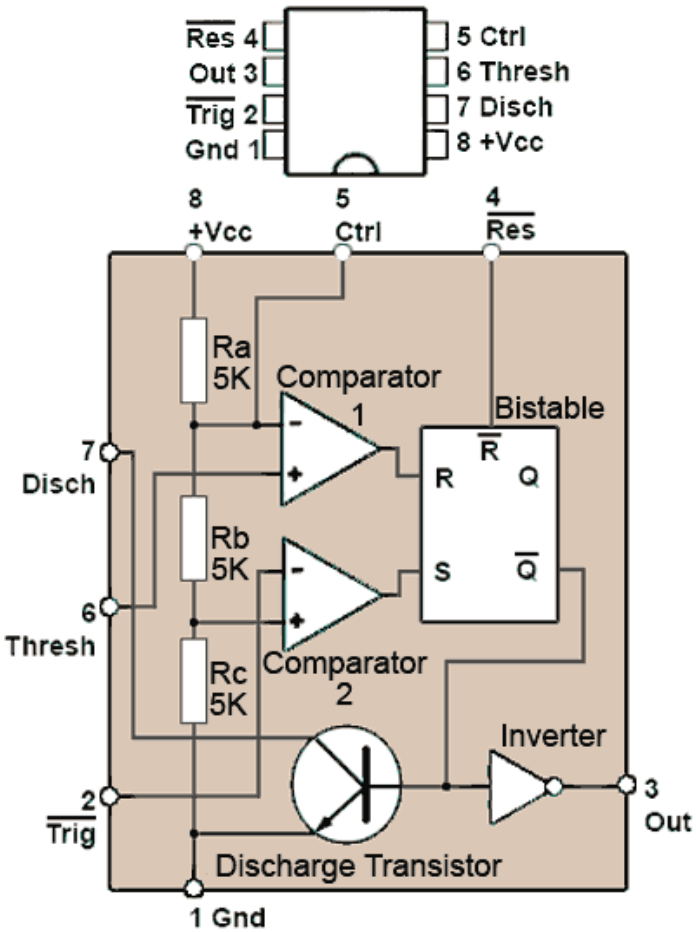

Fig. 4.3.1 The 555 Timer IC

Pin 1. Gnd = Ground connection.

Pin 2. Trig = Trigger (active low).

This active low pin (indicated by the horizontal bar above its name) is normally high (at +Vcc) but when it is momentarily taken low (below 1/3 Vcc) it initiates a sequence of internal events that make the output (pin 3) go high for a period of time set by the value of an external RC time constant.

Pin 3. Out = Output.

The output goes high (to +Vcc) during a time constant period then returns to 0V. When the IC is operated in astable mode two time constants are involved, one governing the high, and one the low condition. The output is capable of sinking and sourcing up to 200mA, which makes it capable of driving a number of commonly used devices such as LEDs, relays, lamps and small motors without the need for external driver stages.

Pin 4. Res = Reset (active low).

Normally high but when taken low makes the Q output of the internal bi-stable to reset to its low state, and Q (the inverse of Q) goes to its high state. This immediately makes the output (pin 3) 0V and also causes the Discharge transistor to discharge the external time constant capacitor. If the Reset pin is taken high again the output stays in its reset (0V) condition until the IC is triggered once more by an input trigger pulse at pin 2. In circuits where reset is not required it is normally connected directly to +Vcc. The reset pin can also be used as an 'Inhibit' control. For example it can be used to prevent the action of an astable oscillator driving a buzzer, until such time as its signal is needed.

Pin 5. Ctrl = Control.

Pin 5 allows for the application of a variable voltage to control the length of time of the RC time constant, and so can be used to vary the frequency and/or the mark to space ratio used in generating the output wave. The higher the voltage on the control pin, the longer the periodic time and the lower the frequency of the astable. This enables the IC to be used for such purposes as frequency modulation, by altering the frequency generated by the 555 in astable mode in response to a changing voltage or low frequency signal applied to the control pin.

With an astable producing an uneven mark to space ratio (i.e. pulses) the control pin can also be used to vary the mark to space ratio and so produce pulse width modulation (PWM). Alternatively, if the output of the 555 in astable mode is a series of very narrow negative going pulses, then applying a modulating signal to the control input can be made to vary the high period between the pulses, effectively producing pulse position modulation.

The control pin can also be used with the 555 in monostable mode to vary the time of the generated delay. When the control pin is not being used for timing control, it is not connected to any external voltage, so to prevent any external noise from entering pin 5 it is decoupled, typically using a capacitor of around 100nF . As pin 5 is connected internally to the junction between Ra and Rb, the voltage on pin 5 when not in active use will be 2/3Vcc.

Pin 6. Thresh = Threshold

In astable mode pin 6 is connected externally to the RC time constant charging capacitor, and so as the capacitor charges, the voltage on pin 6 increases. This causes the voltage on the non-inverting input to Comparator 1, to rise until it reaches the threshold level of 2/3Vcc set by the inverting input of Comparator 1 being connected to the junction between Ra and Rb. Once the voltage on pin 6 reaches 2/3Vcc, Comparator 1 output suddenly changes state and initiates a sequence of events that causes the external time constant capacitor to begin discharging.

Pin 7. Disch = Discharge

Pin 7 is connected to the collector of the discharge transistor, and once the threshold pin has tripped Comparator 1 at the end of the charging period for the external timing capacitor, the discharge transistor conducts, causing the discharge period to commence. During this period the output (pin 3) will be held low until the capacitor has discharged to 1/3Vcc when, in astable mode, the Discharge Transistor will turn off and the charging period will start again. In monostable mode however, the capacitor will be discharged completely to 0V to await another trigger pulse at pin 2.

Pin 8. +Vcc = Positive supply voltage

The 555 is available in a number of variant forms including BJT and CMOS types. Depending on type they can operate from positive supplies ranging from 0.9V to 18V with a current requirement ranging from less than 50µA to 10mA for the chip itself. This current requirement must be added to the current needs of any output device, which will be supplied by the output of the 555 when it is in high mode. This load current can be anything up to 200mA depending on the load.

The 555 Astable Oscillator

As shown in Fig 4.3.2 a basic astable requires only two resistors and two capacitors (not including the external load).

The RC time constant that determines the pulse width and frequency is made up of C1 R1 and R2. Pins 6 and 2 are connected together, pin 4 is connected directly to supply as reset is not being used, and the control input on pin 3 is decoupled with a 100nF capacitor.

To produce a square wave output, with a mark to space ratio approaching 1:1, R2 should be a much higher value than R1. The reason for this is in the way that the 555 works.

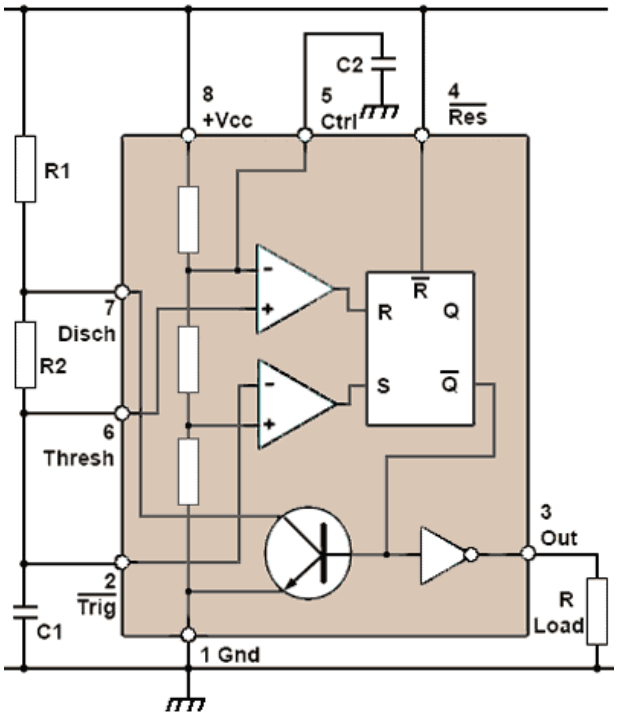

Fig. 4.3.2 The 555 Astable

Astable operation

When power is initially applied to pin 8, capacitor C1 has no charge and so pin 2, the trigger input is active at 0V and C1 begins to charge towards the supply voltage (Vcc) via R1 and R2. As C1 is also connected to pin 6, the voltage on the non-inverting (+) input of comparator 1 also increases. In this condition the output (pin3) will be at Vcc and able to act as a source of current to any load, of up to 200mA.

The inverting (-) input of comparator 1 is connected to the resistor chain Ra, Rb and Rc, which are connected between Vcc and 0V. Since all three resistors have the same value (5K) the voltage on the inverting input will be 2/3Vcc.

So long as the voltage on the non-inverting input of comparator 1 is lower than that on its inverting input, its output will be low (at approximately 0V), but as soon as C1 charges up to 2/3Vcc the comparator will change to its high level (Vcc). This puts a high level on the R (Reset) input of the bistable.

When the R input of the bistable goes high the Q output is reset to zero, and as the (not Q) output is always in the opposite state to the Q output, ‘not Q’ goes high. This has the effect of causing the discharge transistor to conduct heavily and discharge the capacitor C1 via R2. The high voltage on the output of the bistable is also fed to the inverter, which changes this level to a ‘low’ of approximately 0V at the output.

The output of the inverter now allows the output to ‘sink’ up to 200mA.

Once the C1 begins to discharge however, the output of comparator 1 will return to a low level, but this doesn’t matter as the bi-stable will ‘remember’ the very short high pulse delivered to its R input by comparator 1 and will remain in its ‘reset’ state until it receives a similar ‘set’ pulse at its S input.

Notice that when C1 charged, it did so via both R1 and R2, but it now discharges through R2 only. It is for this reason that R1 is made much smaller than R2. If both resistors were equal in value the discharge time (when the output is low) would be half the charge time (when the output is high). By having a ratio of about 100:1 for the values of R2:R1 the mark to space ratio can be made very nearly (but not quite) 1:1.

The falling voltage across C1 is connected to the non-inverting (+) input of comparator 2 so once this voltage falls below that on the inverting (-) input, which it will do at a level of 1/3Vcc, as the inverting input is fed from the top of the lowest resistor Rc in the potential divider resistance chain, the output of comparator 2 will go to its high (Vcc) level. This is fed to the S input of the bi-stable causing the Q and Q output to swap their high and low states, making the output low once more, switching off the discharge transistor and, via the inverter, making the output (pin 3) high.

That completes one whole cycle of the output square wave, and C1 now begins to charge once more towards 2/3Vcc and the cycles repeat as long as power is applied.

Time Constants and the 555

The relationship between the output wave and the charging and discharging of C1 is illustrated in Fig. 4.3.3.

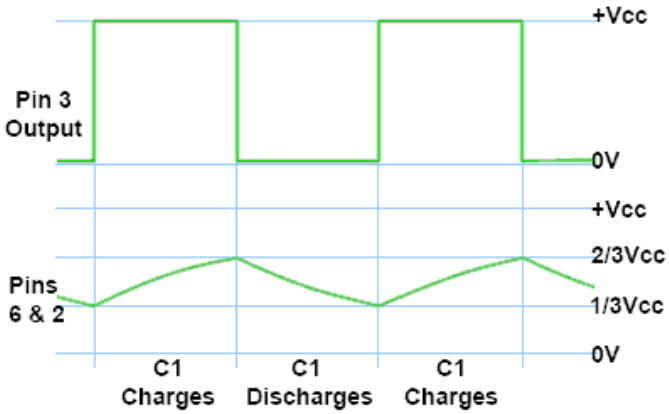

Fig. 4.3.3 Astable Output & Charging Waveforms

The charge time is dependent on the time constant (R1 +R2)C1 and the discharge time is dependent on the time constant R2C1 so the discharge time will always be shorter than the charge time. However when R2 is much greater than R1 the charge and discharge tmes are nearly equal, and for the purpose of calculating the frequency of oscillation R1 may be ignoired, so the period of one cycle is simply the two periods added together.

There is another complication however, the time of the charge or discharge period is not simply the time constant CR because the capacitor is not being allowed to fully charge or discharge, only the central 1/3 of the full charge or discharge is being used, so in calculating the periodic time of the waveform, a constant must be used to modify the normal T = CR time constant formula.

Fig. 4.3.4 illustrates how the time constant formula is modified to make it suitable for calculating the periodic times relating specifically to the 555 astable.

In this example C1 is 50nF and it charges via R1 and R2, which have a combined series resistance of 1MΩ. Therefore the normaltime constant (T = CR) is 50ms and with a supply voltage (Vcc) of 10V, C1 will charge to 3.3V (1/3Vcc) in 20ms and reach 6.67V (2/3Vcc) after 55ms (35ms later).

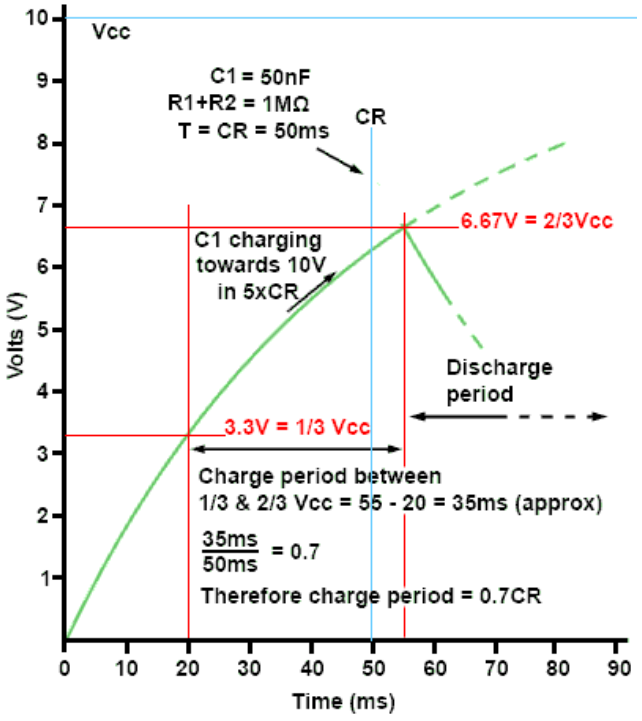

Fig. 4.3.4 The Charge Period of C1

The voltage across C1 would continue to rise to 10V after 5 time constants, except that at 2/3Vcc comparator 1 will switch on (see Fig. 4.3.3) and C1 will begin its discharge period. C1 has therefore charged for only thirty five fiftieths (35/50) or 0.7 of the time constant.

Calculating the Frequency of a 555 Astable

The charge period as C1 charges via R1 andR2 may be calculated as:

Charge (high output) period:

(t_C) = 0.7x(R1+R2)xC1

Because R1 does not play a part in the discharge period this would be calculated as:

Discharge (low output) period:

t_D = 0.7xR2xC1

The periodic time of the whole wave (T) will therefore be:

T = Charge period t_C + Discharge period t_D

so

T = (0.7x(R1+R2)xC1) + (0.7xR2xC1)

Therefore

T =0.7 (R1+2R2) C1

As frequency (f)= 1/T the formula for the frequency of a 555 astable can be written as:

$$f_{osc} = \frac{1}{0.7(R1 + 2R2)C1}$$

And as 1/0.7 = 1.4 the formula for the frequency of a 555 astable can also be written as:

$$f_{osc} = \frac{1.4}{(R1 + 2R2)C1}$$

Oscillators – Module 4
4.4 Designing 555 Astables

What you'll learn in Module 4.4

After studying this section, you should be able to:

- Calculate values of R and C to give an astable of a required frequency.
- Understand methods for varying the duty cycle.
- Understand methods for reducing the effects of noise.

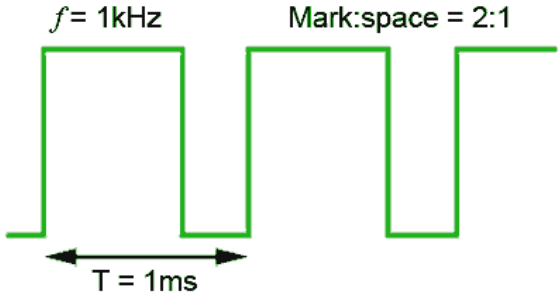

Fig. 4.4.1 Design a 555 Astable to Produce This Wave

Designing 555 Astable Oscillators

If an oscillator of a particular frequency and mark to space ratio is required, (see Fig. 4.4.1) the method would be to calculate periodic time from the required frequency and the discharge time and charge time using the formulae for t_D and t_C described in Oscillators Module 4.3. To do this, some component details will be needed.

Starting with C1, a suitable value can be assumed from the diagram in Fig. 4.4.2, which shows that for an astable having a frequency of 1kHz, and so for a periodic time of 1ms, capacitors of 1nF to 1µF would suffice, depending on which of the total resistances (indicated by the red lines) was chosen.

Manufacturers specify the maximum total resistance that may be used with their particular variant of the 555, and these maximum values are usually around 10 to 20MΩ, however using such high values can increase the error between calculated and actual frequencies, so for many uses a 1MΩ maximum can be recommended. The minimum total resistance value for the combination of R1 and R2 depends largely on the value of R1. The junction of R1/R2 is connected to pin 6 and to the trigger input pin 2. If the value of R1 is less than about 1KΩ, there is a danger that the trigger input may not be able reach a low enough voltage to trigger comparator 1, and so oscillations cannot take place.

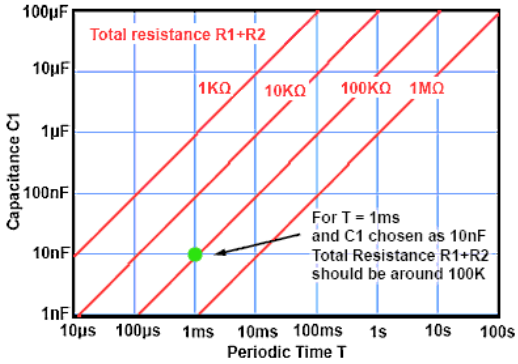

Fig. 4.4.2 Finding Suitable Values for C1

From this it can be assumed that if R1 must be 1KΩ or above and R1 + R2 should be kept below 1MΩ; a 10nF capacitor would allow a suitable total resistance of around 100KΩ to be calculated.

Example

To design a 555 astable with a frequency of 1kHz and a mark to space ratio of 2:1

Periodic time T = 1/f = 1/1000 = 1ms

Charge time t_C = 2/3T = 667µs

Discharge time t_D = 1/3T = 333µs

Assuming (from Fig. 4.4.1) a 10nF capacitor will be used, which discharges via R2 only:

$$t_D = 0.7 \times R2 \times C1$$

Re-arranging the formula to find R2 gives:

$$R2 = \frac{t_D}{0.7 \times C1} = \frac{333\text{exp}^{-6}}{0.7 \times 10\text{exp}^{-9}}$$

$$= \mathbf{47.6K\Omega}$$

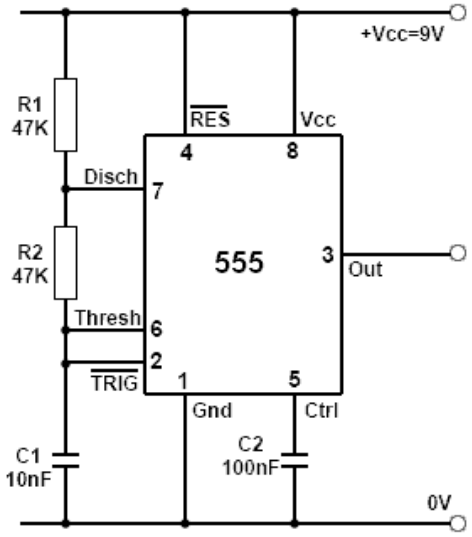

Fig. 4.4.3 555 Circuit for 1kHz 2:1 Mark to Space Ratio

During the charge time C1 charges via R1 + R2, therefore:

$$t_C = 0.7 \times (R1+R2) \times C1$$

Rearranging the formula to find (R1+R2) gives:

$$(R1+R2) = \frac{t_C}{0.7 \times C1} = \frac{667\text{exp}^{-6}}{0.7 \times 10\text{exp}^{-9}}$$

$$= \mathbf{95.3K\Omega}$$

As R1 = (R1+R2) - R2 then:

$$R1 = 95.3K\Omega - 47.6K\Omega = \mathbf{47.7K\Omega}$$

Choosing the nearest preferred values for R1 and R2 gives the value 47KΩ for both resistors.

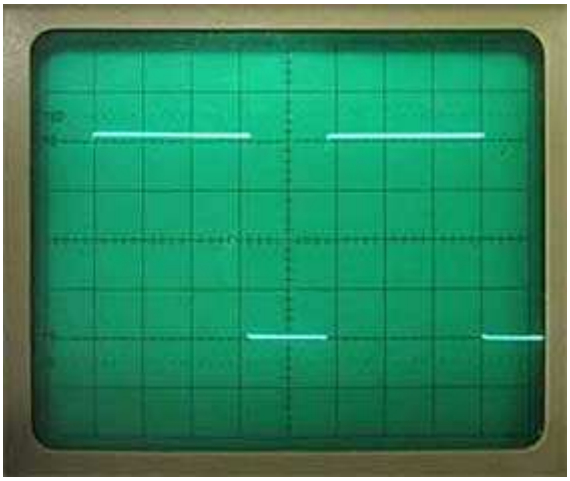

Fig. 4.4.4 Output 1kHz 2:1 Mark to Space Ratio

To check that two 47KΩ will give the required frequency of 1kHz, simply apply the frequency formula for a 555 astable using the calculated values:

$$f_{osc} = \frac{1.4}{(R1 + 2R2)C1}$$

$$f_{osc} = \frac{1.4}{(47\text{exp}^3 + 94\text{exp}^3) \times 10\text{exp}^{-9}}$$

$$= \underline{993\text{Hz (approx 1kHz)}}$$

Mark to Space Ratio

The basic 555 astable design described above uses two timing resistors when producing square waves. In timing the high (charging) period the timing capacitor (C1 in Fig. 4.4.3) is charged via R1 and R2, but only R2 is used whilst discharging C1.

In this basic configuration, the resistance used for timing the high period must always be greater than that used during the low period. The high period of the wave must therefore always be longer than the low period. It follows that the basic version of the 555 astable produces square waves than can be nearly, but never quite 1:1 mark space ratio square waves.

Duty Cycle

The mark to space ratio of a square wave or pulse oscillator is often referred to as the Duty Cycle. This is a more useful term when the purpose of an output wave is to drive some device such as a motor. It gives a more useful comparison to the power supplied to the motor than describing the mark to space ratio of the output. Changing the duty cycle changes the average DC voltage or DC current level of the output, as shown in Fig. 4.4.5 and hence the power supplied to control the speed of the motor. This is also important in driving output devices such as lamps, heaters and many others.

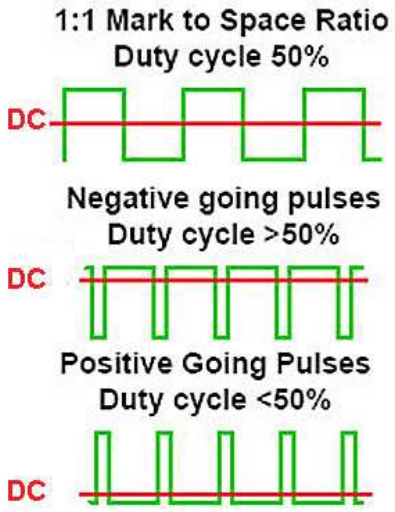

Fig. 4.4.5 The Effect of Duty Cycle on DC Level

The Duty Cycle is a term that describes the percentage of each cycle taken up by the active or high period. For example a square wave with a mark to space ratio of 1:1 has a duty cycle of 50% so the high period takes up 50% of the total period. In the waveform illustrating negative going pulses in Fig. 4.4.5 the duty cycle may be about 80% while in the positive going pulse waveform, the duty cycle may be around 20%.

50% Duty Cycle Astable

Although the basic form of the 555 astable is limited to producing an output with a duty cycle that is always greater than 50%, one of the great benefits of using the 555 timer as an astable oscillator is the ease with which the circuit can be modified to produce a much wider range of duty cycle.

Where a completely symmetrical output wave (50% duty cycle) is required, an alternative method is to use the circuit shown in Fig. 8. In this configuration, shown using the pin-out of the actual 555 IC, the timing capacitor is still connected to pins 2 and 6 as in the basic astable circuit, but a single timing resistor is now connected to the output, pin 3.

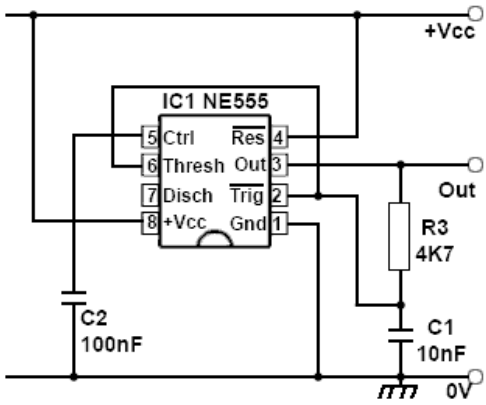

Fig. 4.4.6 One to One Mark to Space Ratio

Operation

During the high period of the waveform C1 charges from the high output via R1 until the voltage at pin 6 reaches 2/3Vcc and triggers comparator 1. The output now goes low and C1 discharges via R1 until the voltage at pin 2 falls to 1/3Vcc when comparator 2 triggers and starts a new charging period. As only one resistor is used for charge and discharge in Fig. 4.4.6 both charge and discharge times are now identical at 0.7CR, which gives a simplified formula for the approximate frequency of oscillation.

$$f_o = \frac{1}{1.4CR} \quad \text{or} \quad f_o = \frac{1.4}{CR}$$

There are however, some drawbacks to this solution for obtaining a 50% duty cycle. Surprisingly the circuit may not always produce a 50% duty cycle. One reason for this is that the design assumes that the output of the 555 changes between 0V and Vcc, but in practice the actual output voltage depends to some extent on the load placed on the output. It is common for example, that in a 555 with a 9V supply the output may change between 0V and just a little over 8V, and with different load resistances, this difference between Vcc and output voltage may again vary.

The trigger points at which the 555 IC switches its output are a fixed proportion of Vcc because they are supplied from the three internal resistors between +Vcc and 0V, but the rate at which the timing capacitor in this design charges now depends, not on Vcc as in the basic design, but on the output voltage. Therefore differences in timing can occur because the voltages at the output pin 3 and at Vcc are not the same, this can affect both the frequency and mark to space ratio. However performance can be improved in a number of ways to make a number of useful circuits.

The 555 Control Input

Pin 5 of the 555 is the Control (Ctrl) pin, which in many applications serves only to decouple the inverting input of comparator 1 inside the IC to prevent noise causing incorrect triggering of the circuit. However, this pin can also function as a useful input, allowing the control of the frequency and duty cycle when the 555 is used in astable mode.

The control input is also connected to the resistor chain in the IC that controls the 2/3 and 1/3Vcc trigger points of the circuit. Therefore by externally applying a DC voltage to pin 5, the internally set trigger points can be altered to lengthen or shorten the charge and discharge periods of the generated wave. Measuring the voltage on pin 5 would normally show a voltage of 2/3Vcc, and applying a higher voltage than this would increase the time of the charge period as the timing capacitor has to now reach this higher voltage before comparator 1 triggers. Therefore the higher the voltage on pin 5 the longer the charge period and the lower the frequency of the wave. Reducing the voltage on pin 5 below its normal 2/3Vcc will cause the charge period to shorten and the frequency to increase.

Pin 5 therefore provides a method of changing the frequency of oscillation by applying a DC voltage, and since pin 5 can still be effectively decoupled by quite a large value of decoupling capacitor, the potentiometer for controlling the frequency can be located some distance from the oscillator without the problem of introducing noise to the circuit.

Varying the Duty Cycle

Fig. 4.4.7 shows how simple control over the duty cycle can be implemented in the basic 555 astable circuit by the use of the control input. A potentiometer VR1 is used to apply a variable voltage to pin 5. The limits of variation is set by R1 and R2 so that the control voltage is not allowed to swing to +Vcc or to 0V, allowing the duty cycle to be adjusted over a range above and below 50%. One problem with using the control pin in this way is that it affects both the duty cycle and the frequency at the same time.

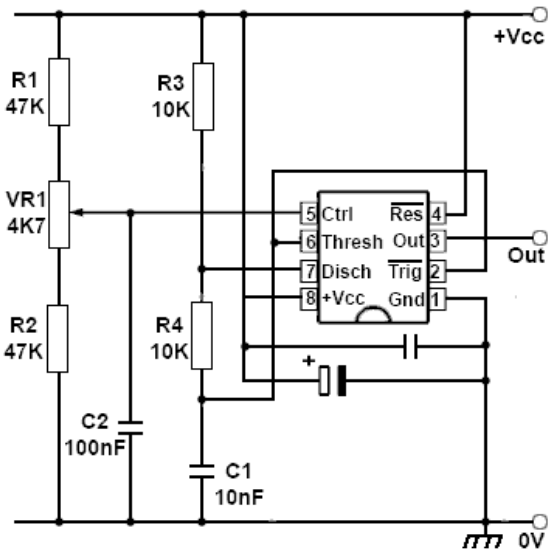

Fig. 4.4.7 Duty Cycle Control Using Ctrl (pin 5)

Improved Duty Cycle Control

A circuit providing an adjustable duty cycle with a minimal effect on frequency is shown in Fig 4.4.8. This is a modified version of the 50% duty cycle circuit shown in Fig. 4.4.6.

VR1 provides a continually adjustable duty cycle between approximately 35% and 75% avoiding use of the control input therefore allowing adjustment of the duty cycle with little or no effect on the frequency of oscillation.

The two sections of VR1, either side of the slider, added to R1 and R2 effectively provide two separate (and adjustable) values of timing resistor. D1 conducts during the charge period of C4 when the output on pin 3 is high, providing a timing resistance made up of R3, the left hand portion of VR1, and R1. During the discharge period pin 3 is low, so D1 is reverse biased; D2 now provides a discharge path via R2, the right hand portion of VR1, and R3.

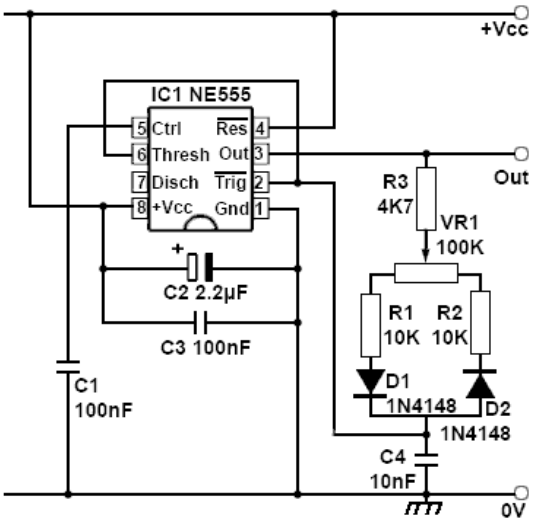

Fig. 4.4.8 Improved Duty Cycle Control

The frequency is calculated using the same formula as for the 50% duty cycle circuit shown in Fig. 4.4.6, although this will be slightly affected by the forward resistance of the diodes:

Also, in this circuit R is now made up of R3 + half of VR1 + R2 (or R1, which is the same value). Frequencies from a fraction of 1Hz to many tens of kHz can be obtained from Fig 4.4.8 by using different combinations of values for the timing capacitor C4 and the timing resistors R1, R2 and R3. To maintain a 1:1 mark space ratio R1 and R2 should be kept equal in value.

Fig 4.4.9 shows the circuit in Fig. 4.4.8 constructed on Breadboard.

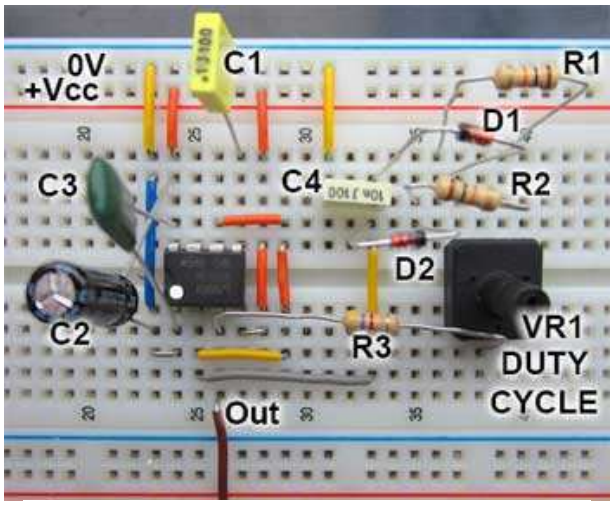

Fig. 4.4.9 555 Astable with Duty Cycle Control

Oscillators – Module 4
4.5 The 555 Monostable

What you'll learn in Module 4.5

After studying this section, you should be able to:

- Understand the operation of the 555 timer in monstable mode.
- Recognise 555 monostable circuits in schematic diagrams.
- Choose appropriate timing components.
- Understand the need for trigger pulse conditioning.

The 555 as a Monostable

The 555 timer is so named because its primary mode of operation is intended to be in monostable mode. Operating as a monostable, it does not fit the strict definition of an oscillator because, unlike true oscillators, it requires an input signal to trigger its operation, however the fact that the 555 timer can be used in both monostable and astable mode considerably increases its flexibility and usefulness.

Monstable Operation

Unlike the astable, which has two unstable states and so continually switches from one to the other and back again, the monstable has one stable state and one unstable state.

When triggered by a suitable pulse at its input (pin 2) it switches from its stable state, in which the output is low, to its unstable state where its output is high. This state exists for a time controlled by the values of R1 and C1, and at the end of this period the output switches back to its stable (low) state. Its primary use is therefore to produce a set time delay, initiated by an input pulse.

From Fig. 4.5.1 it can be seen that the circuit differs from the basic astable configuration shown in Oscillators Module 4.3 in that only one timing resistor (R1) is used, pins 6 and 7 (instead of 6 and 2) are connected together and pin 2 is used for the trigger pulse input.

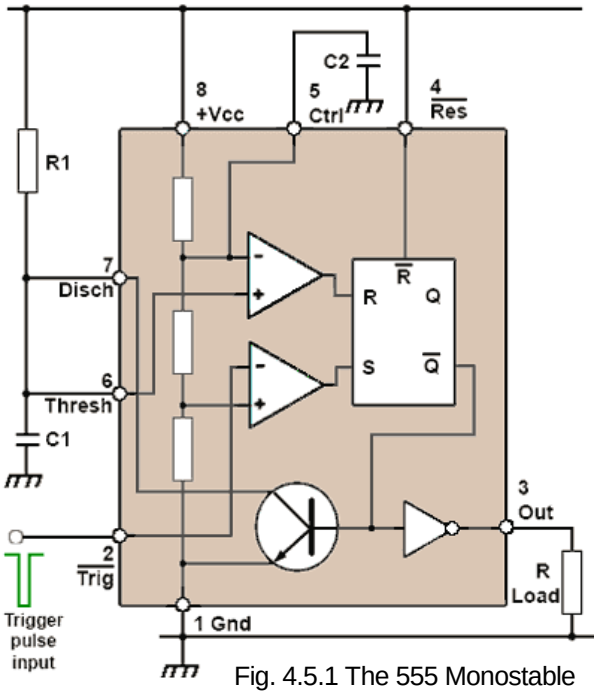

Fig. 4.5.1 The 555 Monostable

Fig. 4.5.2 illustrates the timing waveforms for the monostable, notice that the trigger pulse on pin 2, which must be higher than 1/3Vcc in the absence of a trigger pulse but is normally at about +Vcc, falls to less than 1/3 Vcc to trigger the start of the delay (high output) period.

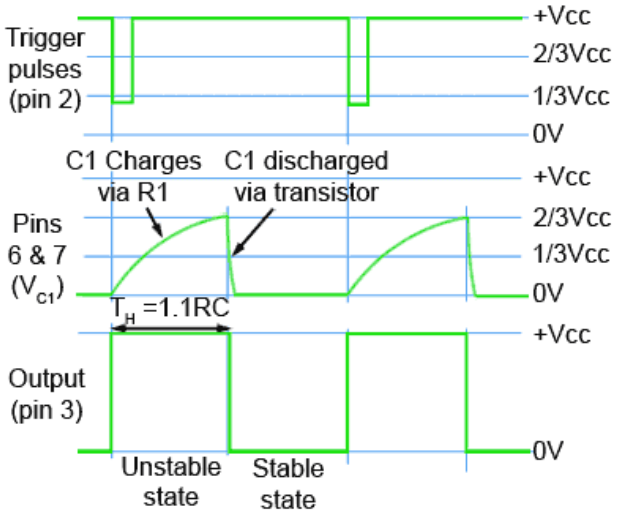

Fig. 4.5.2 555 Monstable Waveforms

The trigger pulse makes the voltage on the inverting input of comparator 2 lower than its non-inverting input and so the comparator output goes high, making the S input of the bistable high and setting the bistable Q output high, and its $\overline{Q}$ (not Q) output low. This turns off the discharge transistor and the low output from the bistable is inverted by the inverter to make the output at pin 3 high.

C1 commences charging from 0V towards +Vcc, but once V_{C1} reaches the discharge level of 2/3Vcc, Comparator 1 is triggered, the bistable is reset, the output at pin 3 goes low and the discharge transistor immediately discharges C1. As C1 is also connected to the non-inverting input of comparator 2, this voltage also falls, and as the trigger voltage on pin 2 is now high again after the trigger pulse, the 1/3Vcc threshold level that was active in the astable configuration is ignored as V_{C1} falls and C1 is fully discharged to 0V. No further action takes place until the arrival of a further trigger pulse at pin 2, and during this time the monostable is said to be in its stable state.

Fig. 4.5.3 shows a schematic diagram for a basic 555 monostable circuit with an output pulse duration of just over 1 second. Because this circuit is not working at high frequencies, the supply decoupling capacitors C3 and C4 may be considered as optional, but nevertheless it is good practice to make sure the circuit is not affected by external noise by decoupling the 555 supply with a 100nF capacitor (to remove high frequency noise) and an electrolytic of around 2 µF (to remove low frequency noise). Both of these capacitors should be fitted as physically close to the 555 IC as possible.

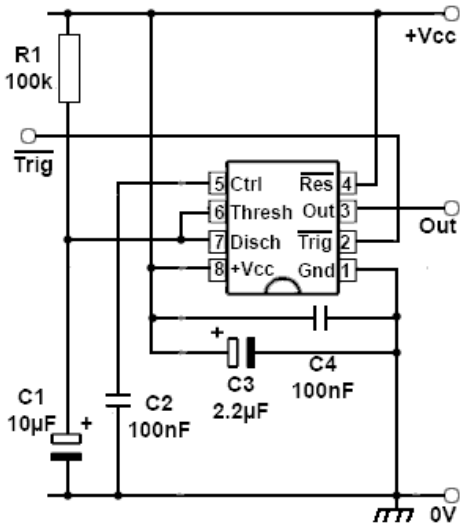

Fig. 4.5.3 555 Monstable Circuit

Timing Components

In monstable mode, only one resistor and one capacitor are involved in the timing process, and as the capacitor charges from 0V to 2/3Vcc in 1.1 time constants, from the information on capacitor time constants,, a capacitor will charge in an exponential fashion to 63.2% of its full charge voltage (+Vcc) in one time constant, so to reach 2/3Vcc (66.7%) will take 1.1 time constants. The delay period (T) is the time taken for the timing capacitor to charge to this level and so can be simply calculated as:

$$T = 1.1 \times RC$$

As the point at which the capacitor begins to discharge is a fraction (2/3) of Vcc, due to the internal resistor chain in the 555, waveform timing is unaffected by changes in the supply voltage.

Choosing a timing capacitor

The 555 monostable can generate delays from a few microseconds to several hours depending on the values or R1 and C1. However, using very large capacitor values can be a problem, since large value electrolytic capacitors have quite wide tolerance limits, so their actual value may not be the same as their value markings by a significant amount. They also have high leakage currents and this can affect the timing accuracy as the capacitor charges. Where large capacitance values must be used, tantalum capacitors can be a better choice due their lower leakage current.

High working voltage electrolytic capacitors should also be avoided where possible as electrolytics do not function properly as capacitors when operated at voltages less than about 10% of their rated working voltage. For example, using an electrolytic capacitor rated at 100Vwkg in a 555 circuit operating on a 5V supply could also cause timing problems. Capacitor working voltages should therefore be chosen that are higher than the 555 +Vcc voltage, so that they can work safely without the danger of an over voltage causing a sudden and catastrophic short circuit in the capacitor, but not so high that they cause timing problems.

Very small value timing capacitors used in producing very short output pulses may also cause problems. If values below 100pF are used, stray capacitance around the circuit can change the value of timing capacitance considerably, leading to inaccurate and unpredictable timing.

WARNING: Be extra careful when connecting electrolytic capacitors to ensure they are connected with the correct polarity, see Fig. 4.5.4 showing negative lead marking on a capacitor, but note that the convention for capacitor symbols in circuit schematic diagrams (e.g. Fig. 4.5.3) is to mark the **positive** plate of an electrolytic capacitor with a + symbol. Fig. 4.5.4 also shows the safe working voltage of the capacitor, which must be high enough to withstand any likely voltage the capacitor will be subject to in the circuit.

Connecting electrolytic capacitors the wrong way round, or exceeding their working voltage can cause them to EXPLODE!

Choosing the timing resistor

As with astables, the timing resistor must be at least 1KΩ (and higher is better if low power consumption is an aim), but if timing inaccuracies are to be minimised, it should not be much higher than 1MΩ.

If timing delays are needed that are longer than can be accommodated by following the above information, it is possible to use multiple monostables, with the falling output of one triggering the next. However an even better (and possibly cheaper) option would be to use digital counters for timing purposes.

Trigger pulses

To trigger the 555, pin 2 must momentarily go to less than 1/3Vcc, the duration of the trigger pulse must not be longer than that of the output pulse, and with short output periods or long duration input (trigger) pulses, some conditioning of the trigger pulse may be needed to keep its duration short. A common method is to differentiate the trigger pulse to produce a very narrow negative going spike at the falling edge of the pulse as shown in Fig. 4.5.5.

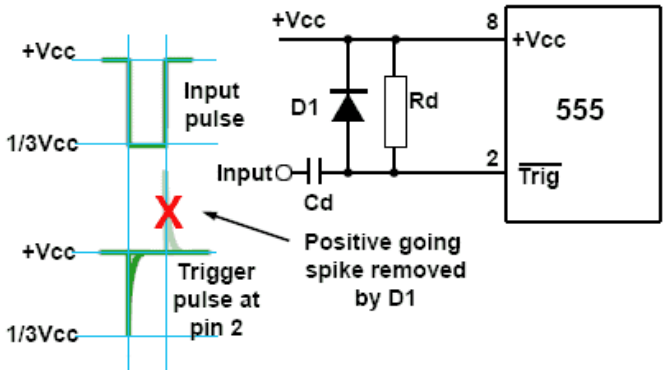

Fig. 4.5.5 Differentiating 555 Trigger Pulses

The differentiator Cd and Rd produces two spikes symmetrical about +Vcc, but as spikes going more positive than +Vcc will not play any part in triggering the 555 and would additionally contribute to unwanted noise in the circuit, they are removed by D1, which will prevent any voltages higher than +Vcc appearing at pin 2.

The result is a much narrower trigger pulse, the duration of which will depend on the values of Rd and Cd. The values of these components are not critical provided that Rd does not load the input too much and reduce the amplitude of the trigger pulse, and that the resulting duration of the trigger pulse (at 1/3Vcc) is less than the duration of the output pulse.

Oscillators – Module 4
4.6 Pulse Width Modulation

What you'll learn in Module 4.6

After studying this section, you should be able to:

- Understand how timer ICs can be used for PWM.
- Know basic methods of pulse width control.
- Apply PWM principles to motor control.
- Understand back EMF protection for inductive loads.

Using Astables & Monostables for Pulse Width Modulation (PWM)

Monostables are widely used in generating simple time delays, an example of which could be the delay in switching off the courtesy light in a car, some seconds after the ignition switch is turned off. There are many other uses however that also make use of the 555 timer's versatility.

In the 555 astable examples shown in Oscillator Module 4.4, the control input (pin5) of the 555 was shown to be useful in controlling the duty cycle of the output. However its action also varied the frequency of the astable. This interdependence can be eliminated by using two 555 timers, the first as a constant frequency astable pulse generator, driving the Trigger input of a second 555 used as a monostable, with its delay timing varied by a voltage applied to its control pin. Such circuits can be constructed using either two 555 timer ICs or a single 556 Dual timer, which is really two 555s in a single package.

In the circuit shown in Fig. 4.6.1 the duty cycle can be adjusted without any effect on the output frequency, making the circuit useful as a pulse width modulated motor speed control or LED dimmer.

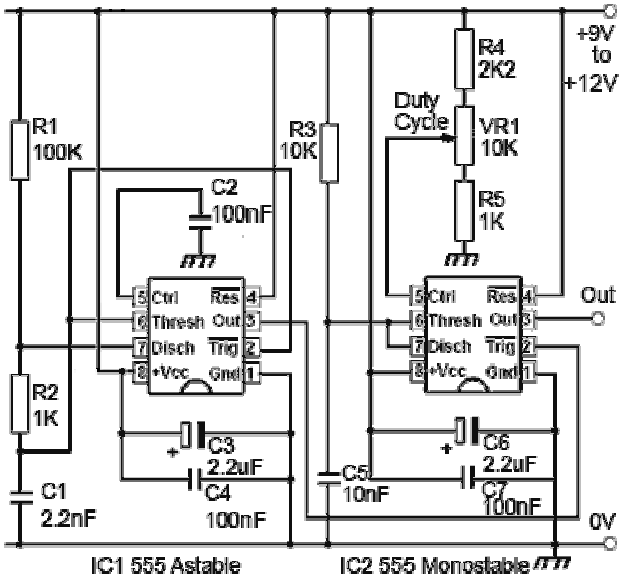

Fig. 4.6.1 Pulse Width Modulation with Astable & Monostable

Operation

IC1 is a fixed frequency (5kHz) astable producing 2µs negative going pulses repeating every 200µs. Each pulse triggers the monostable IC2, to produce a single output pulse giving a high output, of about 110µs set by the values of the timing components R3 and C5. However this time is altered by the variable voltage applied to pin 5 of IC2 by VR1, allowing the delay period to be varied between about 30 and 180µs, i.e. a duty cycle variable between about 15 and 90% as shown in Fig. 4.6.2, these upper and lower limits being set by the values of R4 and R5 respectively.

The monostable period must always be shorter than the time between the astable pulses to ensure that the monostable is not re-triggered before its time-out, as this would cause output pulses of unpredictable duration.

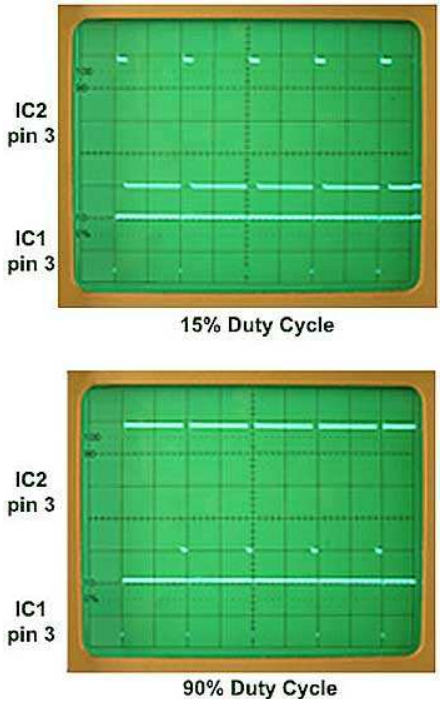

Fig. 4.6.2 Pulse Width Modulation

The narrow negative going pulses produced by IC1 are due to R1 being 100 times greater than R2. The control input (pin 5) of IC1 is not used, and is simply decoupled by C2 to remove any external noise. Both IC1 and IC2 are also externally decoupled by 2.2µF and 100nF capacitors fitted as close to the Vcc and Gnd pins of the ICs as possible. Without this precaution the 555 output can exhibit excessive overshoot at frequencies higher than a few hundred Hz.

Back EMF Protection

The 555 output is capable of sinking or sourcing up to 200mA and so should be quite capable of directly driving small DC motors. However, when connecting inductive loads, such as motors to the 555 output, it is necessary to provide some back e.m.f. protection as shown in Fig. 4.6.3.

For low impedance loads, or if the current drawn by the load is likely to exceed 200mA, a simple emitter follower output driver can be added using a suitable power transistor such as the TIP31A. This will allow output currents up to 3A

If the motor is connected between pin 3 of the 555 and +Vcc, it will be driven whenever the 555 is low. Each time pin 3 goes high, drive current through the motor ceases very suddenly, and a back e.m.f. voltage spike can be produced that will be considerably more positive than +Vcc. Fitting a diode across the motor with its anode to pin 3 will prevent pin 3 going more positive than about 0.7V higher than +Vcc.

When a motor is connected between 3 and ground, it is driven whenever the 555 output goes high. In this case a negative voltage spike will be produced by the motor back e.m.f. each time the 555 output returns low. A protection diode connected with its cathode to pin 3 will limit the amplitude of the back e.m.f. spike across the motor to about –0.6V. However when connecting inductive loads such as motors between pin 3 and ground on a monostable, there is also a risk that even the small 'glitch' produced as the motor is switched off by the 555 output could cause the monostable to re-trigger, effectively doubling the output's high period. To prevent this, a second diode is needed, connected in series with the motor as shown in Fig. 4.6.3. The diodes used for spike suppression should be capable of passing sufficient current for the load and have a considerably higher breakdown voltage than +Vcc so that they are not damaged by the back e.m.f. produced by inductive loads, therefore rectifier diodes such as a 1N4001 should be used.

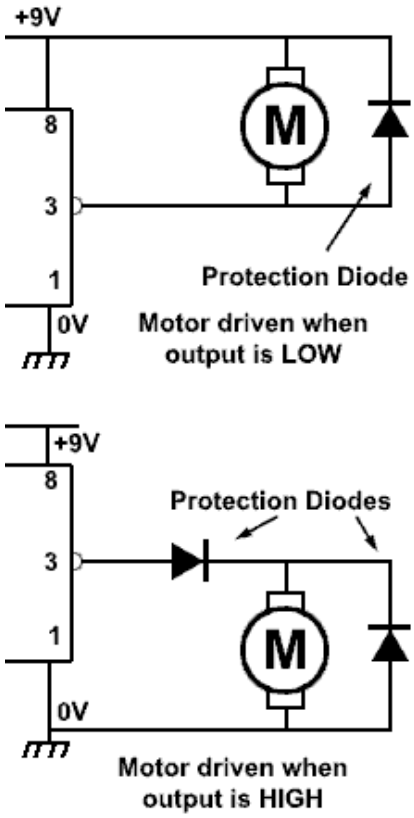

Fig. 4.6.3 Back EMF Protection

Simple Motor Drive Circuit

Fig. 4.6.5 Miniature DC Motor

Although a maximum output current from pin 3 of a standard NE555 (other versions vary) is 200mA, the maximum power dissipation of the 555 is given as 600mW. This would assume that the maximum output voltage was no more than:

$600\exp^{-3}W / 200^{-3}A = 3V$

If a motor is to be driven at a higher voltage, e.g. 9V and the maximum power dissipation of the 555 is to be kept within the 600mW limit either the output current or the output voltage must be limited, for example:

$600\exp^{-3}W / 9V = 67mA$

So even some small DC motors may easily exceed the drive capability of the 555. In such cases a simple drive circuit such as that shown in Fig. 4.6.4 may solve the problem. It consists of a TIP31A NPN power transistor connected in emitter follower mode to the 555 output via a 1K resistor so the 555 has to supply only sufficient current to the base of the transistor to turn it fully on. The transistor will then provide sufficient current via its low impedance emitter output, to drive a motor (or other low impedance devices such as loudspeakers).

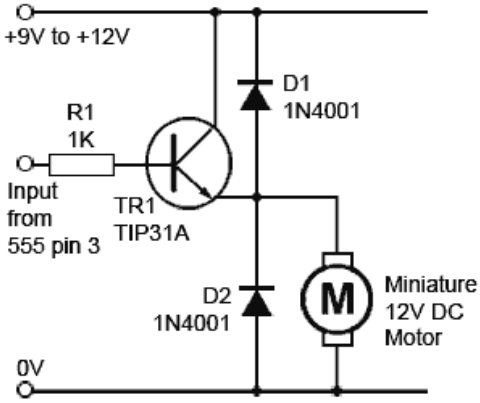

Fig. 4.6.4 Simple Motor Drive Circuit

Because the motor is an inductive load, some protection must be provided for the transistor against high voltage spikes due to back e.m.f. This is achieved by D1, which will conduct if any large positive spike, due to back e.m.f occurs as the motor is switched off. Also D2 will prevent the emitter becoming more negative than 0V, protecting the transistor in the presence of any negative going spikes. This circuit can be added to the circuit in Fig.4.6.1, as shown in Fig. 4.6.6.

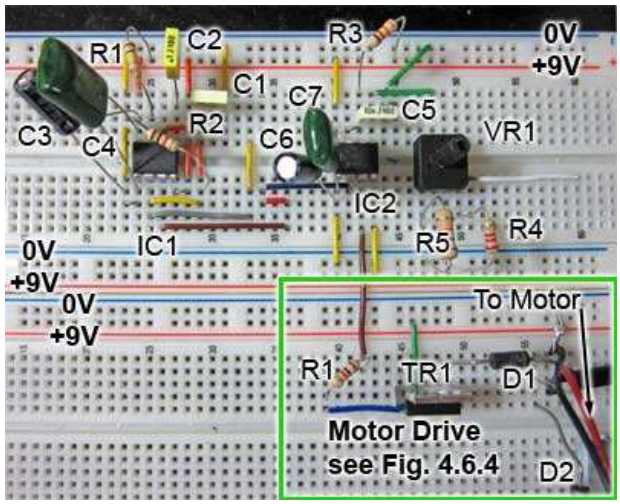

Fig. 4.6.6 Complete PWM Circuit & Motor Drive

4.7 Square Wave Oscillators Quiz

Try our quiz, based on the information you can find in Oscillators Module 4. You can check your answers by using the online version at:

http://www.learnabout-electronics.org/Oscillators/osc47.php

1. What is the duty cycle of a square wave having a mark to space ratio of 2:1

a) 33%

b) 50%

c) 67%

d) 200%

2. What is the p.r.f. of the wave shown in Fig. 4.7.1?

a) 6Hz

b) 60Hz

c) 600Hz

d) 6kHz

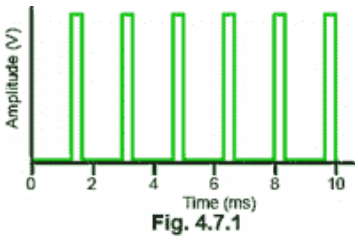

Fig. 4.7.1

3. Refer to Fig. 4.7.2. What is the purpose of D1 and D2?

a) To improve the rise time of the waveform.

b) To eliminate overshoot.

c) To reduce ringing.

d) To clamp the DC level of the waveform.

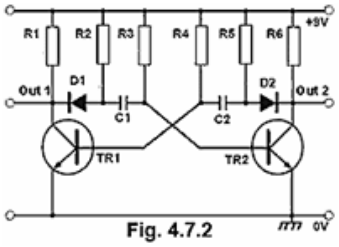

Fig. 4.7.2

4. In the op-amp astable circuit shown in Fig. 4.7.3, which of the following op-amp characteristics limits the highest useful frequency of the circuit?

a) Gain

b) Slew rate

c) Supply voltage

d) Output impedance.

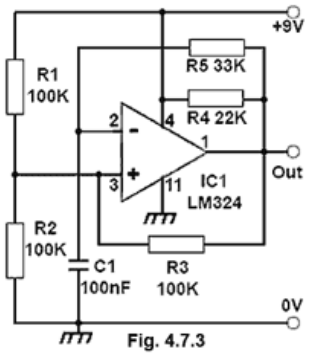

Fig. 4.7.3

5. Refer to Fig. 4.7.3. What is its approximate frequency of oscillation?

a) 220Hz

b) 2.4kHz

c) 50Hz

d) 430Hz

6. Refer to Fig. 4.7.4. Which of the following would be the approximate output frequency?

a) 200Hz

b) 500Hz

c) 1kHz

d) 2kHz

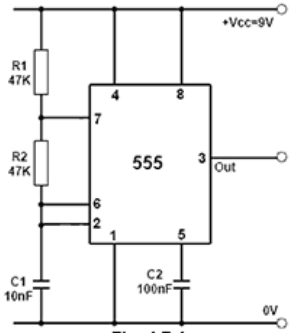

Fig. 4.7.4

7. Refer to Fig. 4.7.4. What will be the mark to space ratio of the output waveform on pin 3 of the 555 timer?

a) 1:1

b) 2:1

c) 3:1

d) 5:1

8. Refer to Fig. 4.7.4. What voltage reading would be expected if a DC voltmeter is connected to Pin 5 of the 555 timer?

a) 0V

b) 3V

c) 6V

d) 9V

9. Refer to Fig 4.7.5. If a 2µs trigger pulse is applied to pin 2, what will be the approximate duration of the output pulse at pin 3?

a) 2µs

b) 20µs

c) 110µs

d) 220µs

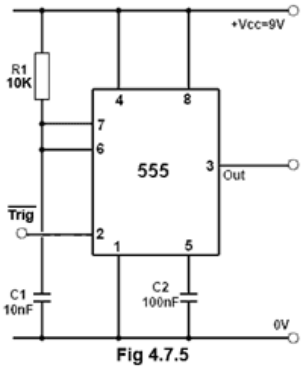

Fig 4.7.5

10. Refer to Fig 4.7.5. To obtain a continuous output waveform with a 50% duty cycle, what would be the required p.r.f. of the repeated trigger pulses applied to pin 2?

a) 4.55kHz

b) 9.1kHz

c) 21kHz

d) 3.25kHz

