

HEF4024B

7-stage binary counter

Rev. 7 — 18 November 2011

Product data sheet

1. General description

The HEF4024B is a 7-stage binary ripple counter with a clock input (\overline{CP}), and overriding asynchronous master reset input (MR) and seven fully buffered parallel outputs (Q0 to Q6). The counter advances on the HIGH to LOW transition of \overline{CP} . A HIGH on MR clears all counter stages and forces all outputs LOW, independent of \overline{CP} . Each counter stage is a static toggle flip-flop.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and benefits

- Tolerant of slow clock rise and fall time
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

3. Applications

- Frequency dividers
- Time delay circuits

4. Ordering information

Table 1. Ordering information

All types operate from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$

| Type number | Package | | Version |
|-------------|---------|--|----------|
| | Name | Description | |
| HEF4024BP | DIP14 | plastic dual in-line package; 14 leads (300 mil) | SOT27-1 |
| HEF4024BT | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |



5. Functional diagram

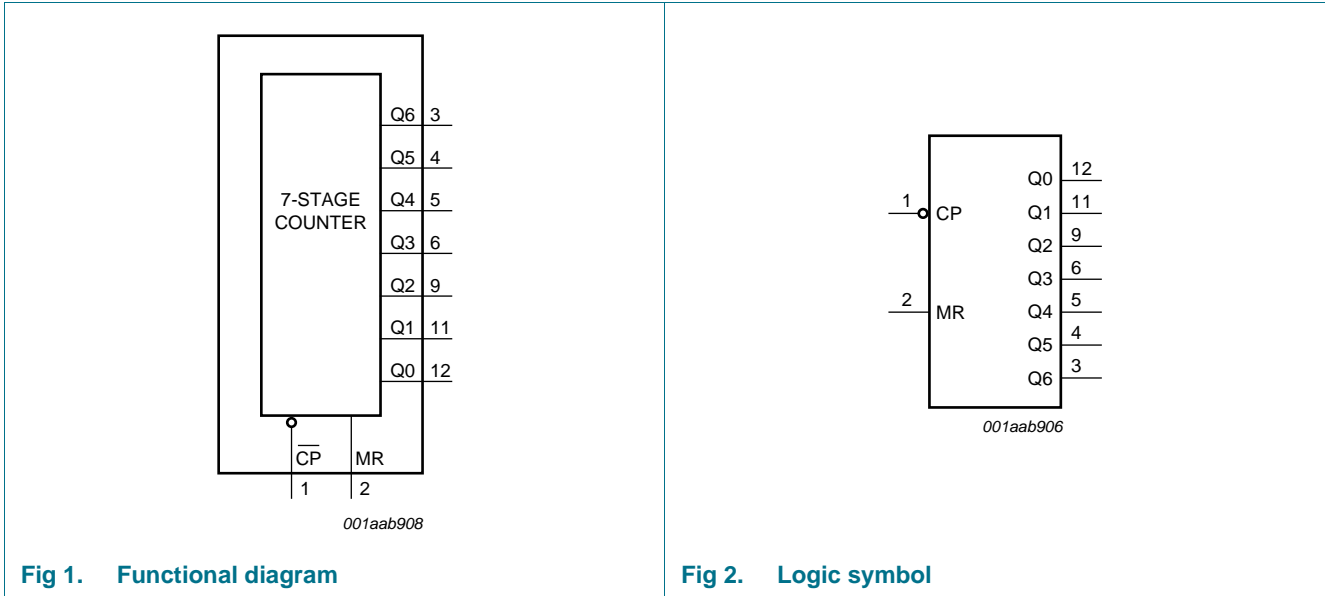


Fig 1. Functional diagram

Fig 2. Logic symbol

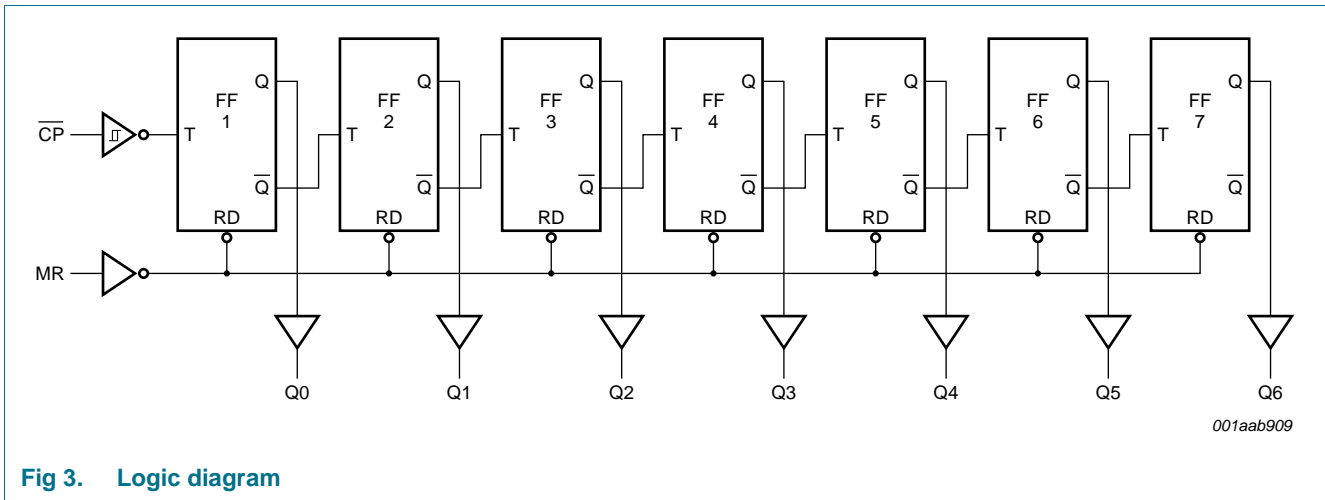


Fig 3. Logic diagram

6. Pinning information

6.1 Pinning

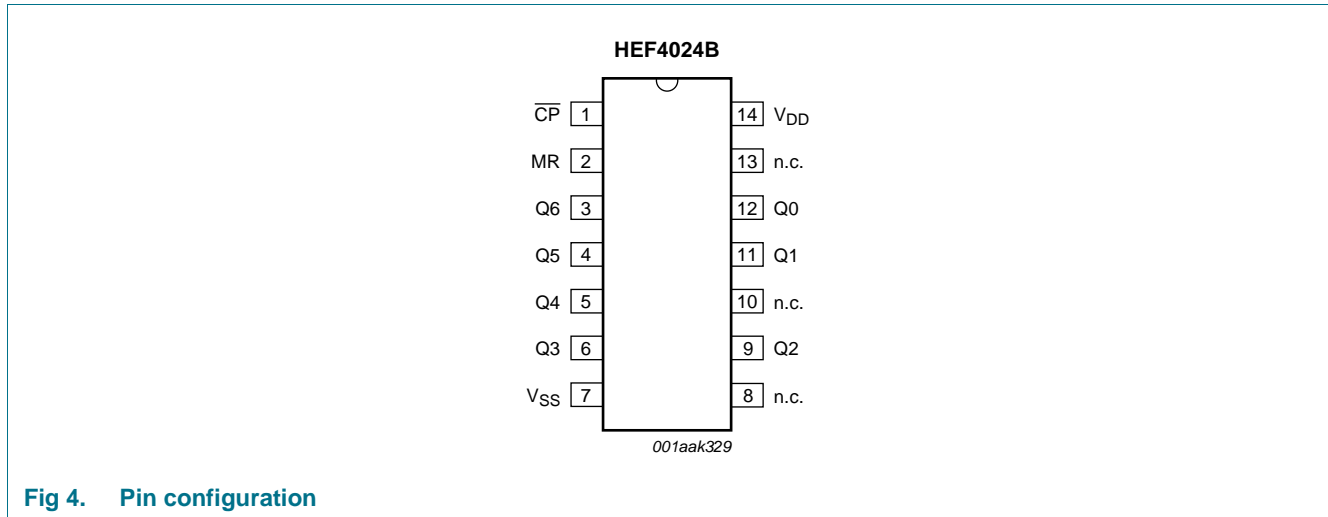


Fig 4. Pin configuration

6.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|------------------------|------------------------|--|
| $\overline{\text{CP}}$ | 1 | clock input (HIGH to LOW edge-triggered) |
| MR | 2 | master reset input |
| V_{SS} | 7 | ground (0 V) |
| n.c. | 8, 10, 13 | not connected |
| Q0 to Q6 | 12, 11, 9, 6, 5, 4, 3, | buffered parallel outputs |
| V_{DD} | 14 | supply voltage |

7. Functional description

Table 3. Functional table^[1]

| Input | | Output |
|------------------------|----|-----------|
| $\overline{\text{CP}}$ | MR | Q0 to Q6 |
| ↑ | L | no change |
| ↓ | L | count |
| X | H | L |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition; ↓ = negative-going transition.

8. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit | |
|-----------|-------------------------|--|------|----------------|------|----|
| V_{DD} | supply voltage | | -0.5 | +18 | V | |
| I_{IK} | input clamping current | $V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$ | - | ± 10 | mA | |
| V_I | input voltage | | -0.5 | $V_{DD} + 0.5$ | V | |
| I_{OK} | output clamping current | $V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$ | - | ± 10 | mA | |
| $I_{I/O}$ | input/output current | | - | ± 10 | mA | |
| I_{DD} | supply current | | - | 50 | mA | |
| T_{stg} | storage temperature | | -65 | +150 | °C | |
| T_{amb} | ambient temperature | in free air | -40 | +85 | °C | |
| P_{tot} | total power dissipation | $T_{amb} -40\text{ °C}$ to $+85\text{ °C}$ | | | | |
| | | DIP14 package | [1] | - | 750 | mW |
| | | SO14 package | [2] | - | 500 | mW |
| P | power dissipation | per output | - | 100 | mW | |

[1] For DIP14 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|-------------------------------------|------------------------|-----|----------|-----------------|
| V_{DD} | supply voltage | | 3 | 15 | V |
| V_I | input voltage | | 0 | V_{DD} | V |
| T_{amb} | ambient temperature | in free air | -40 | +85 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{DD} = 5\text{ V}$ | - | 3.75 | $\mu\text{s/V}$ |
| | | $V_{DD} = 10\text{ V}$ | - | 0.5 | $\mu\text{s/V}$ |
| | | $V_{DD} = 15\text{ V}$ | - | 0.08 | $\mu\text{s/V}$ |

10. Static characteristics

Table 6. Static characteristics
 $V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} ; unless otherwise specified.

| Symbol | Parameter | Conditions | V_{DD} | $T_{amb} = -40\text{ °C}$ | | $T_{amb} = 25\text{ °C}$ | | $T_{amb} = 85\text{ °C}$ | | Unit |
|----------|--------------------------|--------------------------|----------|---------------------------|-----|--------------------------|-----|--------------------------|-----|------|
| | | | | Min | Max | Min | Max | Min | Max | |
| V_{IH} | HIGH-level input voltage | $ I_O < 1\ \mu\text{A}$ | 5 V | 3.5 | - | 3.5 | - | 3.5 | - | V |
| | | | 10 V | 7.0 | - | 7.0 | - | 7.0 | - | V |
| | | | 15 V | 11.0 | - | 11.0 | - | 11.0 | - | V |
| V_{IL} | LOW-level input voltage | $ I_O < 1\ \mu\text{A}$ | 5 V | - | 1.5 | - | 1.5 | - | 1.5 | V |
| | | | 10 V | - | 3.0 | - | 3.0 | - | 3.0 | V |
| | | | 15 V | - | 4.0 | - | 4.0 | - | 4.0 | V |

Table 6. Static characteristics ...continued
 $V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} ; unless otherwise specified.

| Symbol | Parameter | Conditions | V_{DD} | $T_{amb} = -40\text{ }^\circ\text{C}$ | | $T_{amb} = 25\text{ }^\circ\text{C}$ | | $T_{amb} = 85\text{ }^\circ\text{C}$ | | Unit |
|----------|---------------------------|--------------------------------|----------|---------------------------------------|-----------|--------------------------------------|-----------|--------------------------------------|-----------|---------------|
| | | | | Min | Max | Min | Max | Min | Max | |
| V_{OH} | HIGH-level output voltage | $ I_O < 1\text{ }\mu\text{A}$ | 5 V | 4.95 | - | 4.95 | - | 4.95 | - | V |
| | | | 10 V | 9.95 | - | 9.95 | - | 9.95 | - | V |
| | | | 15 V | 14.95 | - | 14.95 | - | 14.95 | - | V |
| V_{OL} | LOW-level output voltage | $ I_O < 1\text{ }\mu\text{A}$ | 5 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 10 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 15 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| I_{OH} | HIGH-level output current | $V_O = 2.5\text{ V}$ | 5 V | - | -1.7 | - | -1.4 | - | -1.1 | mA |
| | | $V_O = 4.6\text{ V}$ | 5 V | - | -0.52 | - | -0.44 | - | -0.36 | mA |
| | | $V_O = 9.5\text{ V}$ | 10 V | - | -1.3 | - | -1.1 | - | -0.9 | mA |
| | | $V_O = 13.5\text{ V}$ | 15 V | - | -3.6 | - | -3.0 | - | -2.4 | mA |
| I_{OL} | LOW-level output current | $V_O = 0.4\text{ V}$ | 5 V | 0.52 | - | 0.44 | - | 0.36 | - | mA |
| | | $V_O = 0.5\text{ V}$ | 10 V | 1.3 | - | 1.1 | - | 0.9 | - | mA |
| | | $V_O = 1.5\text{ V}$ | 15 V | 3.6 | - | 3.0 | - | 2.4 | - | mA |
| I_I | input leakage current | | 15 V | - | ± 0.3 | - | ± 0.3 | - | ± 1.0 | μA |
| I_{DD} | supply current | $I_O = 0\text{ A}$ | 5 V | - | 20 | - | 20 | - | 30 | μA |
| | | | 10 V | - | 40 | - | 40 | - | 60 | μA |
| | | | 15 V | - | 80 | - | 80 | - | 120 | μA |
| C_I | input capacitance | | - | - | - | - | 7.5 | - | - | pF |

11. Dynamic characteristics

Table 7. Dynamic characteristics
 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; for test circuit see [Figure 6](#); unless otherwise specified.

| Symbol | Parameter | Conditions | V_{DD} | Extrapolation formula ^[1] | Min | Typ | Max | Unit |
|-----------|-------------------------------|---|----------|---|-----|-----|-----|------|
| t_{PHL} | HIGH to LOW propagation delay | CP @ Q0; see Figure 5 | 5 V | $73\text{ ns} + (0.55\text{ ns/pF})C_L$ | - | 100 | 200 | ns |
| | | | 10 V | $29\text{ ns} + (0.23\text{ ns/pF})C_L$ | - | 40 | 75 | ns |
| | | | 15 V | $17\text{ ns} + (0.16\text{ ns/pF})C_L$ | - | 25 | 50 | ns |
| | | Qn \rightarrow Qn + 1; see Figure 5 | 5 V | $33\text{ ns} + (0.55\text{ ns/pF})C_L$ | - | 60 | 120 | ns |
| | | | 10 V | $14\text{ ns} + (0.23\text{ ns/pF})C_L$ | - | 25 | 50 | ns |
| | | | 15 V | $12\text{ ns} + (0.16\text{ ns/pF})C_L$ | - | 20 | 40 | ns |
| | | MR \rightarrow Qn; see Figure 5 | 5 V | $93\text{ ns} + (0.55\text{ ns/pF})C_L$ | - | 120 | 240 | ns |
| | | | 10 V | $34\text{ ns} + (0.23\text{ ns/pF})C_L$ | - | 45 | 90 | ns |
| | | | 15 V | $22\text{ ns} + (0.16\text{ ns/pF})C_L$ | - | 30 | 60 | ns |
| t_{PLH} | LOW to HIGH propagation delay | CP @ Q0; see Figure 5 | 5 V | $78\text{ ns} + (0.55\text{ ns/pF})C_L$ | - | 105 | 210 | ns |
| | | | 10 V | $34\text{ ns} + (0.23\text{ ns/pF})C_L$ | - | 45 | 85 | ns |
| | | | 15 V | $22\text{ ns} + (0.16\text{ ns/pF})C_L$ | - | 30 | 60 | ns |
| | | Qn \rightarrow Qn + 1 see Figure 5 | 5 V | $23\text{ ns} + (0.55\text{ ns/pF})C_L$ | - | 50 | 100 | ns |
| | | | 10 V | $9\text{ ns} + (0.23\text{ ns/pF})C_L$ | - | 20 | 40 | ns |
| | | | 15 V | $7\text{ ns} + (0.16\text{ ns/pF})C_L$ | - | 15 | 30 | ns |

Table 7. Dynamic characteristics ...continued
 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; for test circuit see [Figure 6](#); unless otherwise specified.

| Symbol | Parameter | Conditions | V _{DD} | Extrapolation formula ^[1] | Min | Typ | Max | Unit |
|------------------|-------------------|--|--------------------|--------------------------------------|-----|-----|-----|------|
| t _t | transition time | see Figure 5 | 5 V ^[2] | 10 ns + (1.00 ns/pF)C _L | - | 60 | 120 | ns |
| | | | 10 V | 9 ns + (0.42 ns/pF)C _L | - | 30 | 60 | ns |
| | | | 15 V | 6 ns + (0.28 ns/pF)C _L | - | 20 | 40 | ns |
| t _w | pulse width | CP HIGH; minimum width see Figure 5 | 5 V | | 60 | 30 | - | ns |
| | | | 10 V | | 30 | 15 | - | ns |
| | | | 15 V | | 20 | 10 | - | ns |
| | | MR HIGH; minimum width see Figure 5 | 5 V | | 80 | 40 | - | ns |
| | | | 10 V | | 35 | 20 | - | ns |
| | | | 15 V | | 25 | 15 | - | ns |
| t _{rec} | recovery time | MR; see Figure 5 | 5 V | | 20 | 10 | - | ns |
| | | | 10 V | | 15 | 5 | - | ns |
| | | | 15 V | | 15 | 5 | - | ns |
| f _{max} | maximum frequency | CP input; J = K = HIGH; see Figure 5 | 5 V | | 5 | 10 | - | MHz |
| | | | 10 V | | 13 | 25 | - | MHz |
| | | | 15 V | | 18 | 35 | - | MHz |

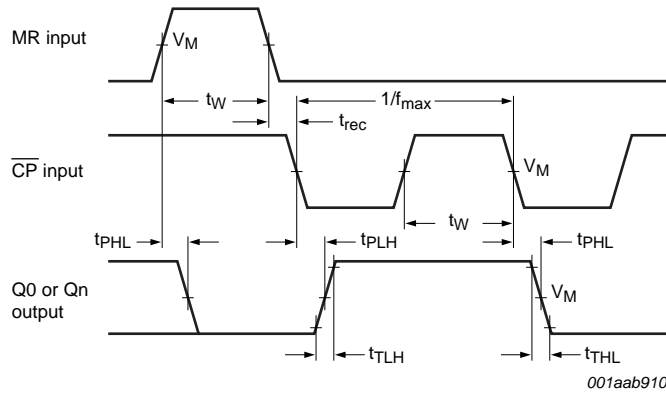
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

[2] t_t is the same as t_{TLH} and t_{THL}.

Table 8. Dynamic power dissipation P_D
P_D can be calculated from the formulas shown. $V_{SS} = 0\text{ V}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ °C}$.

| Symbol | Parameter | V _{DD} | Typical formula for P _D (μW) | Where: |
|----------------|---------------------------|-----------------|--|---|
| P _D | dynamic power dissipation | 5 V | $P_D = 500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | f _i = input frequency in MHz; |
| | | 10 V | $P_D = 2100 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | f _o = output frequency in MHz; |
| | | 15 V | $P_D = 5200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | C _L = output load capacitance in pF; |
| | | | | V _{DD} = supply voltage in V; |
| | | | | Σ(f _o × C _L) = sum of the outputs. |

12. Waveforms

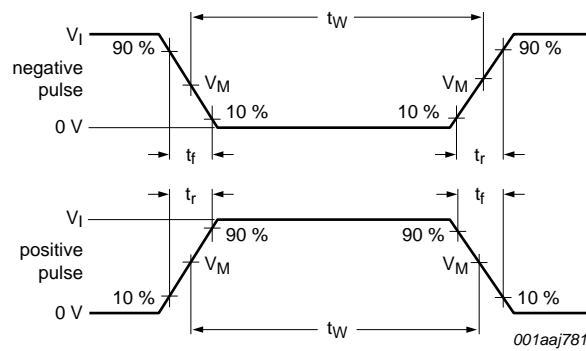


V_{OH} and V_{OL} are typical output voltages levels that occur with the output load.
 Measurement points are given in [Table 9](#).

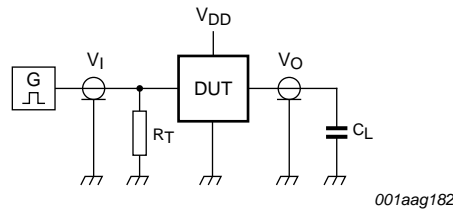
Fig 5. Waveforms showing propagation delays for MR to Qn and CP to Q0, minimum MR and CP pulse widths and recovery time for MR.

Table 9. Measurement points

| Supply voltage | Input | Output |
|----------------|-------------|-------------|
| V_{DD} | V_M | V_M |
| 5 V to 15 V | $0.5V_{DD}$ | $0.5V_{DD}$ |



a. Input waveforms



b. Test circuit

Test data is given in [Table 10](#).

Definitions for test circuit:

DUT = Device Under Test.

C_L = load capacitance including jig and probe capacitance.

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig 6. Test circuit for measuring switching times

Table 10. Test data

| Supply voltage | Input | | Load |
|----------------|----------------------|--------------|-------|
| V_{DD} | V_I | t_r, t_f | C_L |
| 5 V to 15 V | V_{SS} or V_{DD} | ≤ 20 ns | 50 pF |

13. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

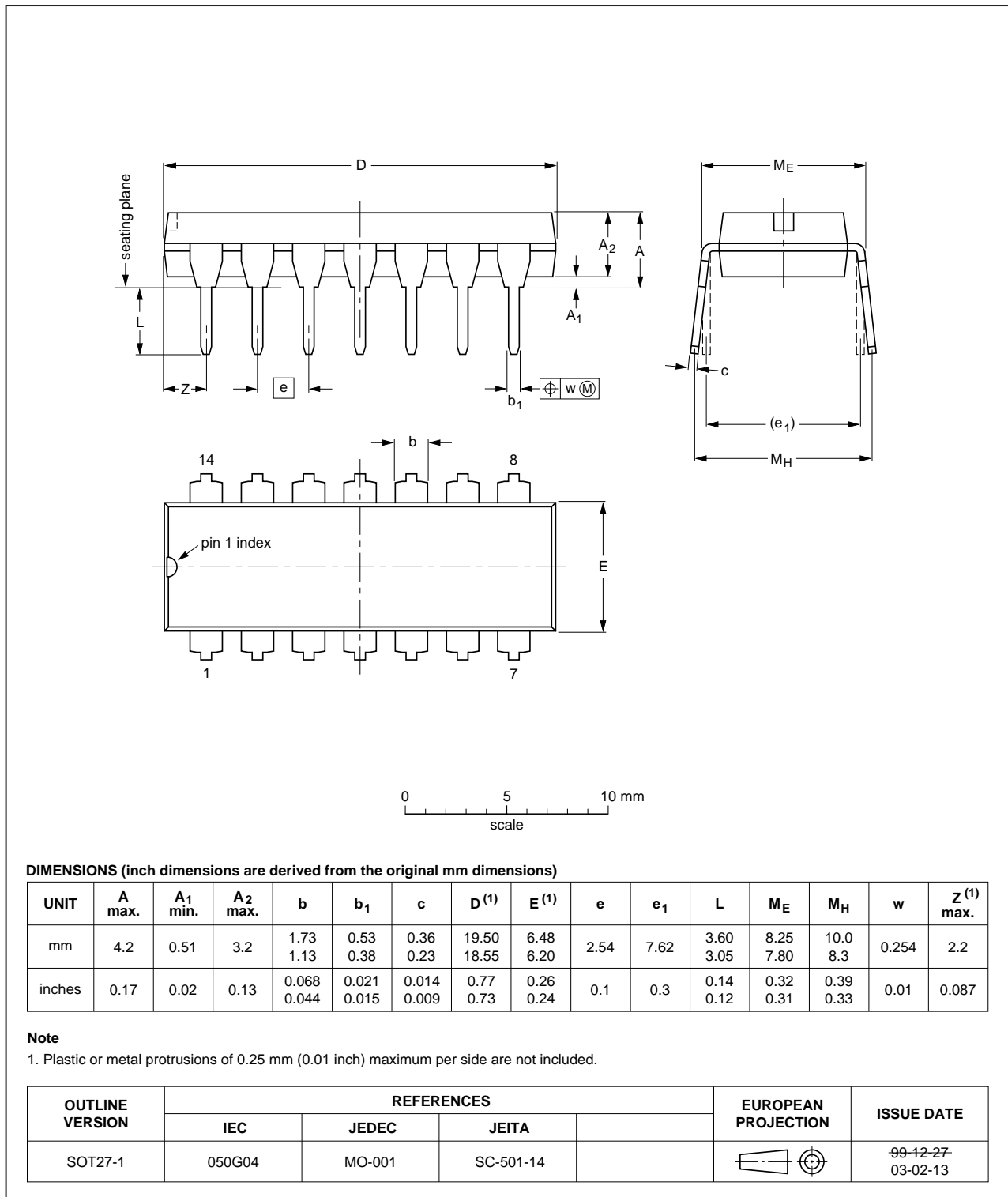


Fig 7. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

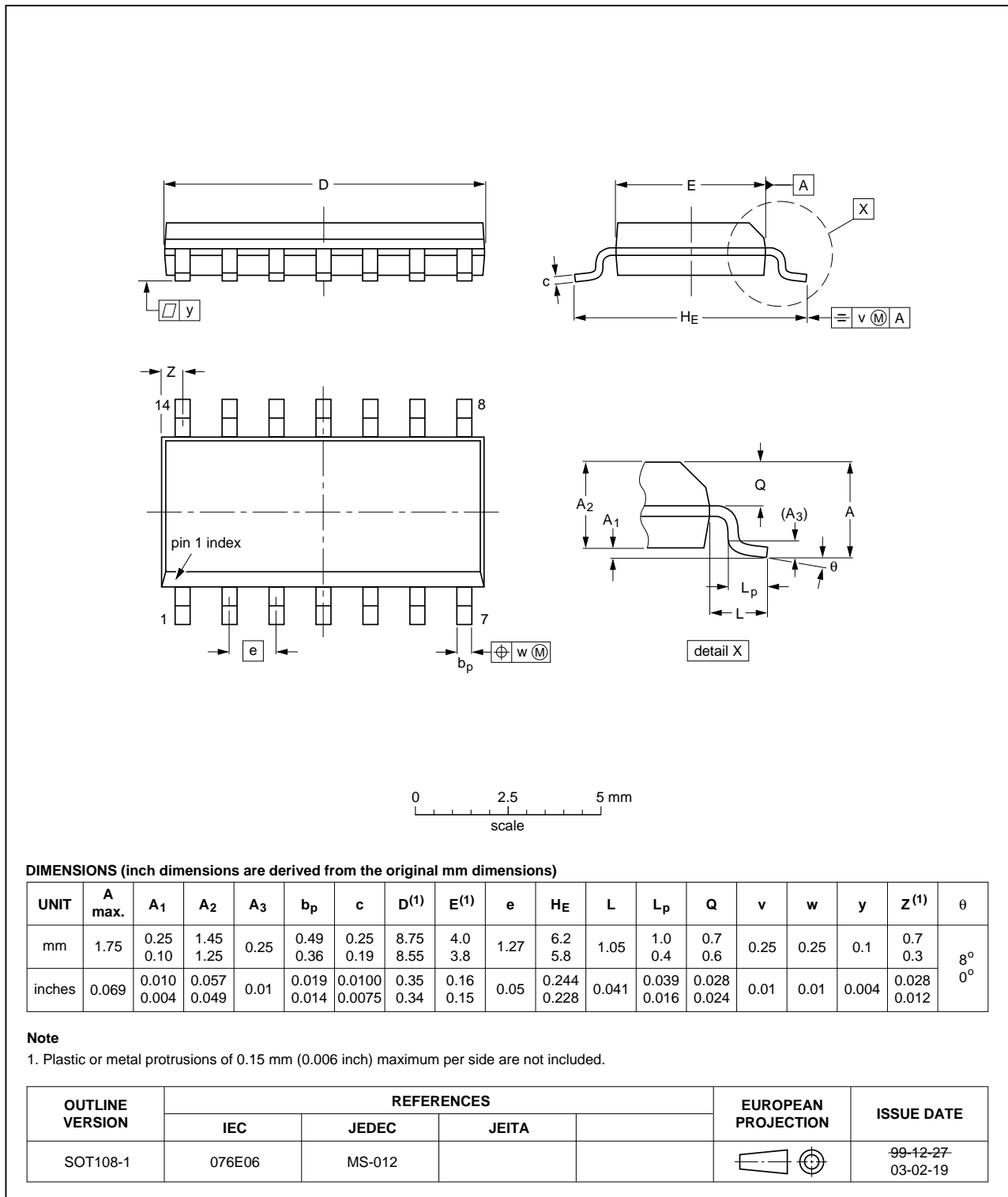


Fig 8. Package outline SOT108-1 (SO14)

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------|--------------|---|---------------|------------------|
| HEF4024B v.7 | 20111118 | Product data sheet | - | HEF4024B v.6 |
| Modifications: | | <ul style="list-style-type: none">• Legal pages updated.• Changes in “General description” and “Features and benefits”.• Table 1, description below table title: +125 °C changed to +85 °C. | | |
| HEF4024B v.6 | 20111010 | Product data sheet | - | HEF4024B v.5 |
| HEF4024B v.5 | 20091109 | Product data sheet | - | HEF4024B v.4 |
| HEF4024B v.4 | 20090902 | Product data sheet | - | HEF4024B_CNV v.3 |
| HEF4024B_CNV v.3 | 19950101 | Product specification | - | HEF4024B_CNV v.2 |
| HEF4024B_CNV v.2 | 19950101 | Product specification | - | - |

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15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
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[2] The term 'short data sheet' is explained in section "Definitions".

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17. Contents

| | | |
|------|--|----|
| 1 | General description | 1 |
| 2 | Features and benefits | 1 |
| 3 | Applications | 1 |
| 4 | Ordering information | 1 |
| 5 | Functional diagram | 2 |
| 6 | Pinning information | 3 |
| 6.1 | Pinning | 3 |
| 6.2 | Pin description | 3 |
| 7 | Functional description | 3 |
| 8 | Limiting values | 4 |
| 9 | Recommended operating conditions | 4 |
| 10 | Static characteristics | 4 |
| 11 | Dynamic characteristics | 5 |
| 12 | Waveforms | 7 |
| 13 | Package outline | 9 |
| 14 | Revision history | 11 |
| 15 | Legal information | 12 |
| 15.1 | Data sheet status | 12 |
| 15.2 | Definitions | 12 |
| 15.3 | Disclaimers | 12 |
| 15.4 | Trademarks | 13 |
| 16 | Contact information | 13 |
| 17 | Contents | 14 |

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